# V.I.R.U.S Multiple Controller Readout Sequence

The following describes the multiple controller readout sequence as executed in the CarcPCIeMux::Expose() method of the CArcSys library.

1. Broadcast "**read controller id's**" to determine the number of controllers connected to each PCIe board. The number of controllers per PCIe board is used to determine the total pixel count expected per PCIe board and is used later in the expose sequence. The actual id values are not used here.

2. '**Initialize Image Address**' by writing a 1 to the **PCIe** register at offset 0x54. No reply is expected.

3. '**Set Pixel Count**' on the **PCIe** board by writing the total number of expected pixels to register 0x50 on the PCIe board. The total pixel count is determined by multiplying the VIRUS image size ( 4096x1024 ) times the total number of connected controllers as determined by step 1. No reply is expected.

4. Broadcast '**AES**' ( Await Exposure Start ) to ALL **controllers**. A 'DON' is expected from all controllers.

5. Send '**SEX**' ( Start Exposure ) to ALL **MUX** boards. The MUX designated as "master", via jumper settings on the board, will return a 'DON' on success; all others will return 'ERR'.

6. The VDAS ( computer ) now waits out the **exposure time** using a software timer.

7. Send '**EEX**' ( End Exposure ) to ALL **MUX** boards. The MUX designated as "master", via jumper settings on the board, will return 'DON' on success; all others will return 'ERR'.

8. Send '**RDA**' ( Read Array ) to ALL **MUX** boards to enable "image mode" instead of "command mode". No reply is expected.

9. Write a 1 to the PCIe register 0x58 to set the **PCIe** board into "**Image Mode**". No reply is expected.

10. Loop over the expected **pixel count**. Reading the current pixel value from the PCIe register 0x70. On error, the PCIe and MUX are set back to "command mode" using steps 11 and 12, and 'ABR' ( Abort Readout ) is broadcast to all controllers. 'ABR' expects a 'DON'.

11. Write a 0 to the **PCIe** register 0x58 to **disable "image mode"** and restore the PCIe board to "command mode". No reply is expected.

12. Send '**COM**' ( Command ) to ALL **MUX** boards to disable "image mode" and restore "command mode". No reply is expected.