Updating CCD voltages remotely in the VIRUS CCD controller

The CCD clocking and DC bias voltages in individual controllers can be changed remotely once the default software is downloaded to all controllers. Individual controllers or a range of controllers are addressed with their controller IDs entered in the command headers, as described below. It works by writing a digital value to an addressed register within a selected DAC. The 'SBN' command is used to select which voltage is to be updated to what value.

'SBN' 'CLK' or 'VID' Address Value

'SBN' is the Set Bias Number command
'CLK' as the second argument selects a clock driver voltage to be updated, whereas 'VID' selects a DC bias or video offset value to be written to the video processor board.
Address is an integer selected from the list below.
The 14-bit Value is written to the selected address of the selected DAC. The conversion formula of this 14-bit integer to voltage or video offset is listed below.

The clock driver board addresses go from 0 to 31 to select the high and low voltages of each of the 16 signals on the ARC-13 clock driver board. The voltage generating circuits are linear bipolar over the range of -13 to +13 volts, operating from 8-bit DACs. The voltage V is

$$V = (\text{Value}/255) \times 26 \text{ volts} - 13 \text{ volts}$$

The table of clock voltage names and address is defined in the file entitled "VIRUS.waveforms" as follows:

Address	Clock driver voltage name	Address	Name
0	Reset Gate High, side A	16	Summing Well High, side A
1	Reset Gate Low, side A	17	Summing Well Low, side A
2	Reset Gate High, side B	18	Summing Well High, side B
3	Reset Gate Low, side B	19	Summing Well Low, side B
4	Serial phase #1 High, side A	20	Parallel phase #1 High, side A
5	Serial phase #1 Low, side A	21	Parallel phase #1 Low, side A
6	Serial phase #2 High, side A	22	Parallel phase #2 High, side A
7	Serial phase #2 Low, side A	23	Parallel phase #2 Low, side A
8	Serial phase #3 High, side A	24	Parallel phase #3 High, side A
9	Serial phase #3 Low, side A	25	Parallel phase #3 Low, side A

10	Serial phase #1 High, side B	26	Parallel phase #1 High, side B
11	Serial phase #1 Low, side B	27	Parallel phase #1 Low, side B
12	Serial phase #2 High, side B	28	Parallel phase #2 High, side B
13	Serial phase #2 Low, side B	29	Parallel phase #2 Low, side B
14	Serial phase #3 High, side B	30	Parallel phase #3 High, side B
15	Serial phase #3 Low, side B	31	Parallel phase #3 Low, side B

The video board addresses go from 0 to 15 to select the DC voltages generated by the ARC-14V video board. The first four circuits each generate a video offset voltage that is subtracted from the voltage input to the A/D converter, so an increased offset value results in a decrease in the image counts.

Address	CCD channel name	Address	CCD channel name
0	Lower left, side A	2	Lower left, side B
1	Upper right, side A	3	Upper right, side B

The next eight circuits generate unipolar DC bias voltages, the first four running from 0 to 30 volts and the next four running from 0 to 20 volts.

Address	DC bias name	Address	DC bias name
4	Output drain lower, side A	8	Reset drain, side A
5	Output drain upper, side A	9	Reset drain, side B
6	Output drain lower, side B	10	Preamp power lower, side A
7	Output drain upper, side B	11	Preamp power upper, side A

The last four circuits generate bipolar DC bias voltages over the range of -10 to +10 volts. They are assigned as follows:

Address	DC bias name	Address	DC bias name
12	Output gate, side A	14	Preamp power lower, side B
13	Output gate, side B	15	Preamp power upper, side B