VIRUS
Detector System
Specification

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1 Introduction

The Hobby-Eberly Telescope (HET) is an innovative large telescope of 9.2 meter aperture, located in West Texas at the McDonald Observatory (Figure 1). A major upgrade of the HET is in progress that will substantially increase its capabilities. This includes development and deployment of a revolutionary new integral field spectrograph called VIRUS (the Visual Integral-Field Replicable-Unit Spectrograph), in support of the Hobby-Eberly Telescope Dark Energy Experiment (HETDEX). VIRUS consists of up to 192 simple fiber-fed spectrographs, each of which contains a camera that employs a cryogenically cooled 2064 x 2064 pixel Charge Coupled Device (CCD).

Figure 1: The HET at McDonald Observatory.

This document contains the requirements for the VIRUS detector system (referred to as the detector system) which consists of the spectrograph CCDs, CCD controller(s) with data acquisition computer interface, power supplies, and associated interconnects. Installation of VIRUS on HET is anticipated to occur in the first quarter of 2011 with science operations commencing in late 2011.

1.1 VIRUS Overview

1.1.1 VIRUS Prototype

VIRUS consists of up to 192 simple fiber-fed spectrographs. A prototype spectrograph (referred to as VIRUS-P) was fabricated and has been in use since October 2006, primarily on McDonald Observatory's 2.7 m Harlan J. Smith Telescope (see Figure 2) for a pilot survey to study the properties of Lyman-α Emitting (LAE) galaxies which are the focus of the HETDEX survey. Later, in March 2008, it was installed on the HET for the first time to verify predicted sensitivities. Tests conducted with VIRUS-P have yielded excellent data which have been used to confirm the adequacy of the design and to test the data reduction and analysis algorithms. Additional tests are underway to obtain data necessary to finalize the design parameters for the spectrographs that will be deployed on the HET (referred to as the VIRUS production spectrographs).

Details associated with VIRUS-P are presented in this section of the document as background material. Later, in Section 2, a reference design is presented which is consistent with the detector system requirements contained in Sections 3 through 13.

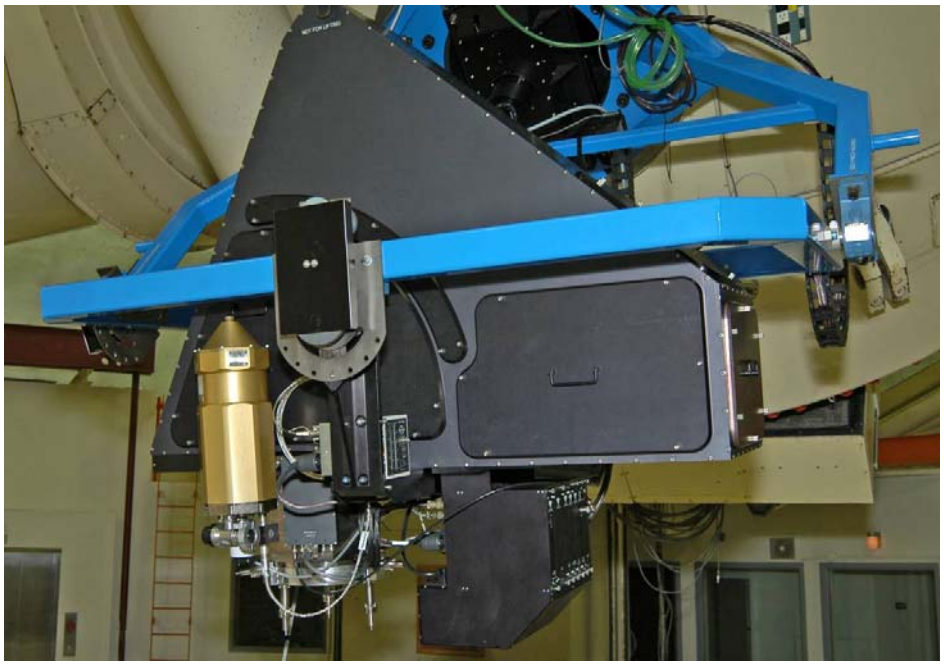

Figure 2: Photograph of VIRUS-P installed on the Harlan J. Smith telescope.

Figure 3 is a view of VIRUS-P with its side cover removed to show the location of its primary components. A detailed description of VIRUS-P can be found in References 1 and 2.

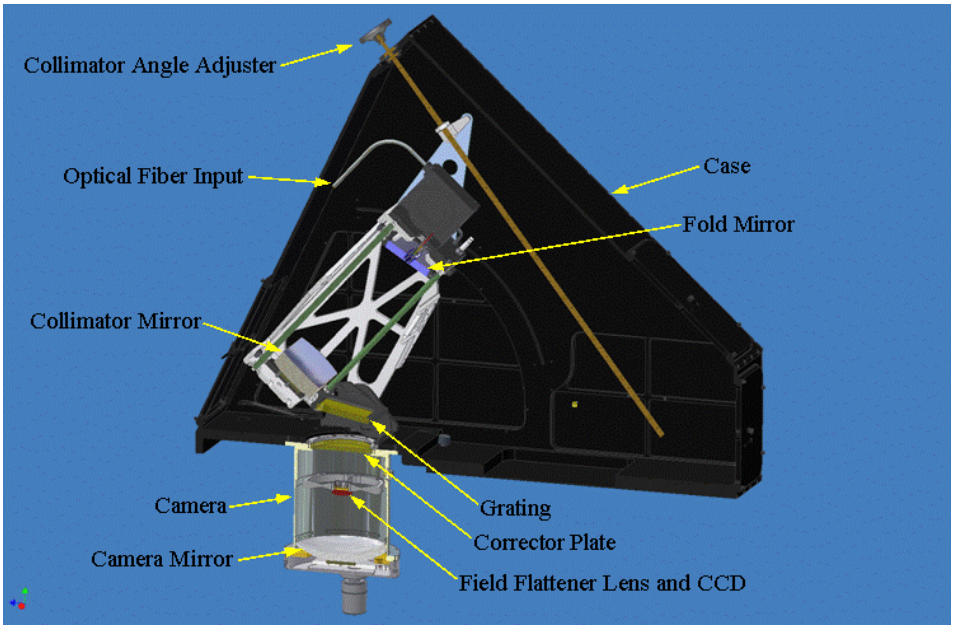

Figure 3: Illustration depicting VIRUS-P's primary components.

The spectrograph camera is located at the bottom of the instrument and is shown in more detail in Figure 4. It is a Schmidt design with the detector at the internal focus. Dispersed light enters the camera through the corrector plate which also acts as the entrance window for the camera's vacuum cryostat housing. Light passing through the corrector plate reflects off the camera mirror, travels through the fused silica Field Flattener (FF) lens, and is detected by the CCD which is located directly behind the FF lens. The FF lens and CCD are suspended in the optical beam (causing an approximate 23% obstruction in area, on axis) as part of the spider assembly (Figures 5 and 6).

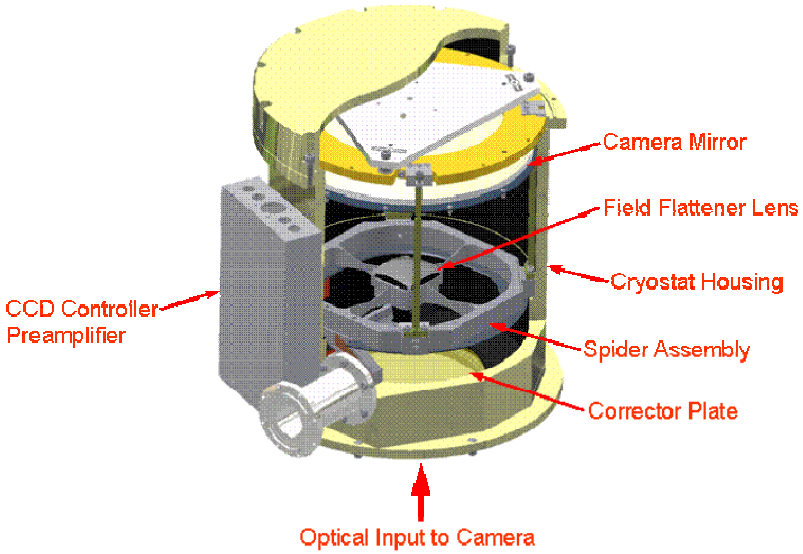

Figure 4: Cutaway close up view of the spectrograph camera showing the location of the spider assembly and CCD controller preamplifier. Note that in this view the camera is upside down with respect to its orientation as shown in Figure 3.

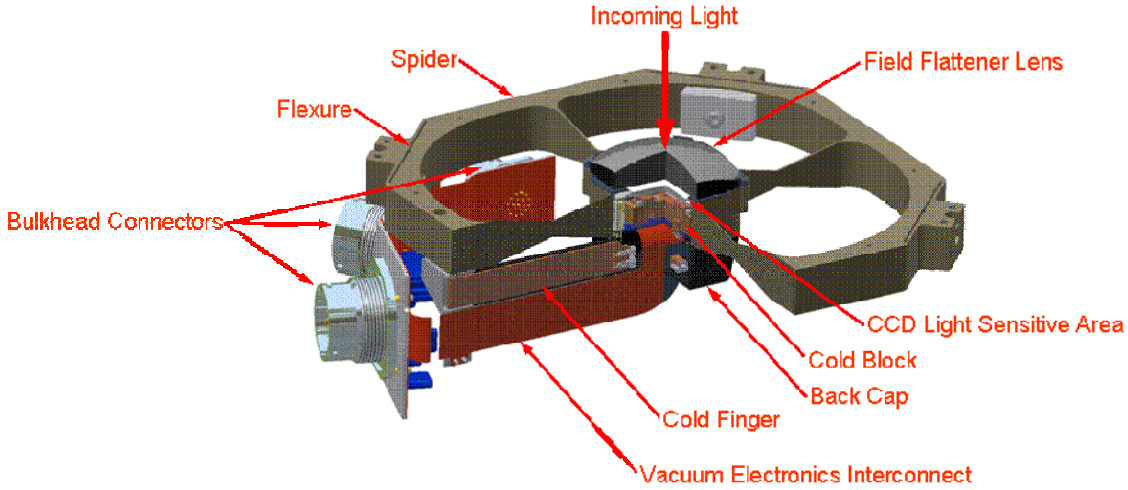

Figure 5: Cutaway close up view of the spider assembly. Flexures incorporated into the spider decouple the expansion of the aluminum cryostat housing from the stainless steel spider.

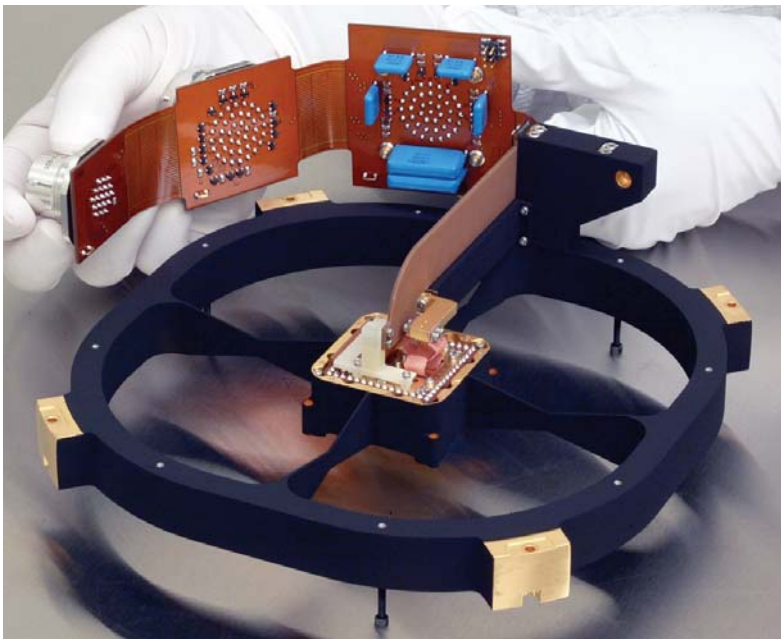

Figure 6: Photograph of the spider assembly with CCD back cap removed. Note that the CCD light sensitive area is facing down in this photograph.

Liquid Nitrogen (LN) is used to cool the CCD to -110°C as shown schematically in Figure 7. The CCD is attached to the cold block which acts as a thermal reservoir. A thermally conductive grease at the CCD/cold block interface enhances the heat transfer between the CCD and cold block. Heat transfer between the cold block and cold finger is via a tuned cold link constructed from copper braid. The CCD and cold block are thermally isolated from the ambient environment with a high vacuum (approximately 10^{-7} mbar), gold-plated surfaces as required to reduce radiative heat transfer, a thermal insulator which is fabricated from Ultem, and a low thermal conductivity electrical interconnect.

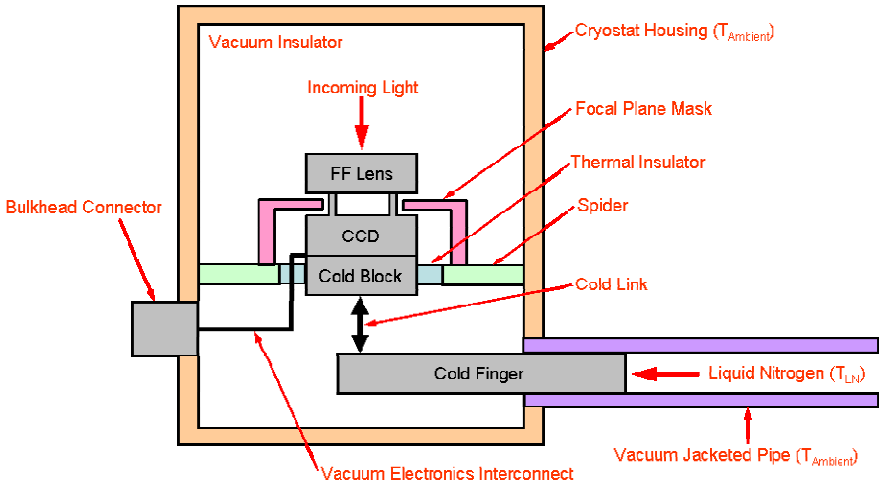

Figure 7: Liquid Nitrogen is used to cool the CCD.

The cold block is equipped with a heater and temperature sensor that is operated closed loop to help maintain the cold block and CCD at an approximately constant temperature (Figure 8).

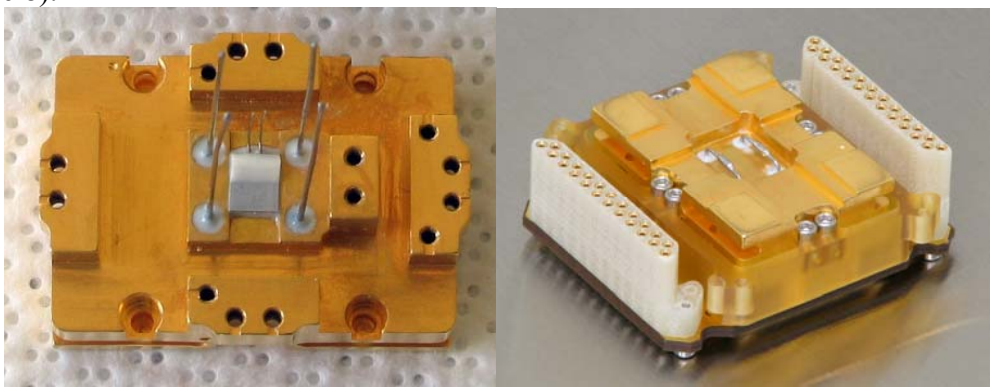

Figure 8: The photograph on the left shows the underside of the cold block which is equipped with a platinum Resistance Temperature Detector (RTD) and four heater resistors. The photograph on the right shows the top side of the cold block that is in thermal contact with the CCD. Note that each pair of resistors is connected in series.

The electrical interconnect between the controller and CCD/heater/temperature sensor is referred to as the vacuum electronics interconnect (Figure 9). It consists of a flex circuit equipped with stiffeners, passive electronics components, and three bulkhead connectors that attach to the cryostat housing. The CCD controller preamplifier is located (nearby) outside the cryostat housing (see Figure 4) and attaches to one of the bulkhead connectors via a cable that is equipped with a quick disconnect. The other two bulkhead connectors (for temperature control and the clock signals) are connected to modules in the CCD controller which is also located outside the cryostat housing.

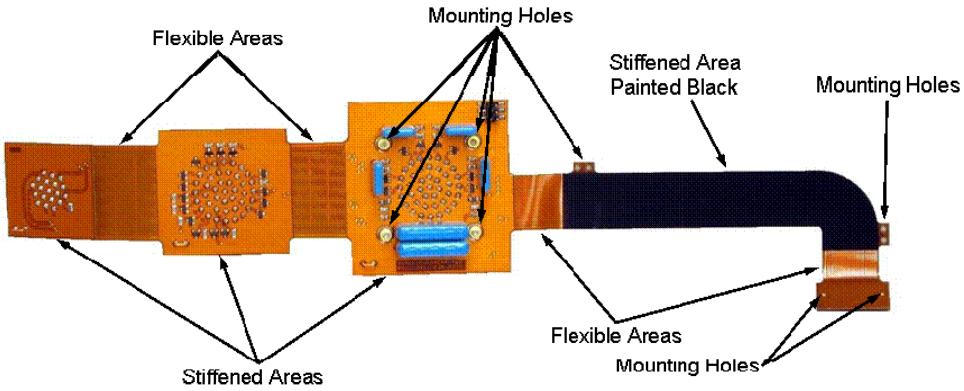

Figure 9: Bottom side of the vacuum electronics interconnect showing the location of the flexible and stiffened areas. The bulkhead connectors are attached to the other side of the interconnect. The stiffened area that is painted black spans the gap between the CCD and cryostat wall. It is painted with ALION MH2200 to control stray light.

The CCD is a Fairchild 3041 detector with 2064 x 2064 15 μm pixels with a 100% fill factor. Read noise with this system is measured as 4.2 electrons at 100 kpxl/s and 3.6 electrons at 25 kpxl/s. The McDonald Observatory Version 2 CCD controller is used on the prototype. This is a very versatile, general-purpose controller, which has substantially more capability than is required for the VIRUS production spectrographs.

A focal plane mask is provided to control stray light (Figure 10). It is mounted close to the CCD and contains a square opening that is slightly larger than the CCD's light sensitive area. Its primary purpose is to absorb stray photons that would otherwise reflect off the portions of the CCD silicon die and substrate that are outside the field of view.

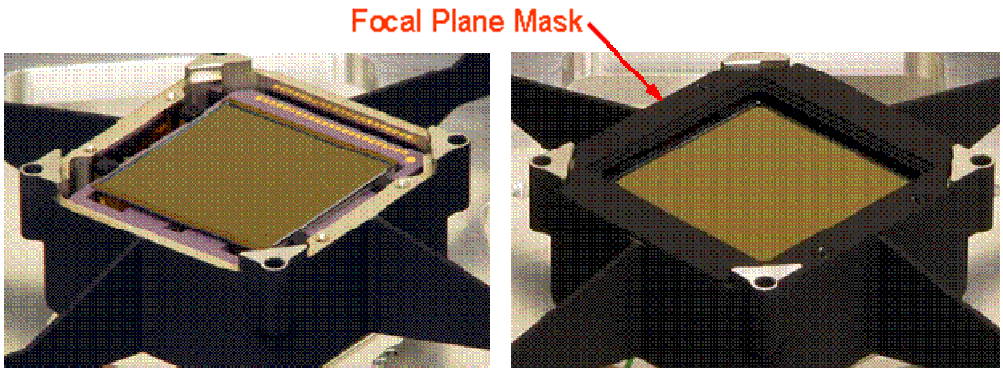

Figure 10: A focal plane mask is provided to control stray light. The photograph on the left shows the spider assembly without the mask. The photograph on the right shows the spider assembly with the mask installed.

1.1.2 VIRUS Preproduction Model

Evolution of the VIRUS design from the prototype to the production model will be made in two steps. First, a preproduction prototype (VIRUS-PP) will be developed that incorporates the value engineering required to reduce costs. After VIRUS-PP performance is validated on the sky, minor changes may be made before production begins with an initial batch of ten units. We do not anticipate that any changes will be made to the detector system (which is specified in this document) as we transition from the VIRUS-PP design to the production model design.

Many design changes have already been made to the spectrograph design based upon experience with VIRUS-P and engineering issues discovered while refining the design of the other HET upgrade components. These include:

- Pairing the spectrographs so that they share a single fiber feed, a single housing, and a common cryostat (left side of Figure 11)
- Modifying the optical layout to make the system more linear, thereby allowing the spectrographs to be packed more efficiently in less space (right side of Figure 11)
- Mounting the spectrographs inside climate-controlled enclosures (referred to as the spectrograph enclosures) that are located closer to the base of the telescope (Figure 12).

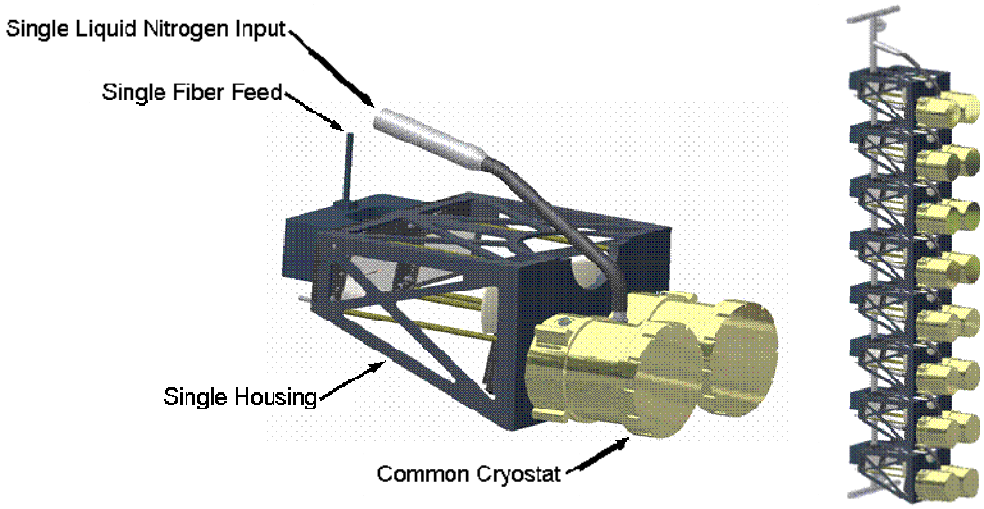

Figure 11: The improved design is simpler, facilitates tighter packing, and reduces costs associated with vacuum valves and gauges. The illustration on the left is a close-up of a spectrograph pair. The illustration on the right depicts the close packing of eight spectrograph pairs.

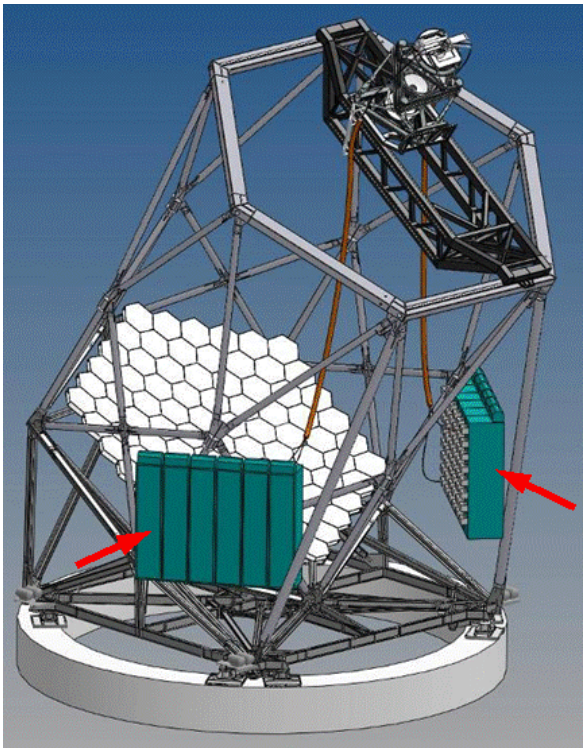

Figure 12: The spectrographs will be mounted inside two climate-controlled enclosures (as indicated by the red arrows) that are located several meters above the base of the telescope.

1.2 Applicable Documents

1) *Mechanical Design of VIRUS-P for the McDonald 2.7 m Harlan J. Smith Telescope*, Michael Smith, Gary Hill, Phillip MacQueen, Werner Altmann, John Goertz, John Good, Pedro Segura, Gordon Wesley, Proc. SPIE, 7014, 701472 (2008)
2) *VIRUS-P: Camera Design and Performance*, Joseph Tufts, Phillip MacQueen, Michael Smith, Pedro Segura, Gary Hill, Robert Edmonston, Proc. SPIE, 7021, 702109 (2008)
3) HX0003 − *Acronyms*, Richard Savage
4) ASME Y14.5M-1994, *Dimensioning and Tolerancing* or equivalent
5) NFPA 70, 2008, *National Electric Code* or equivalent
6) US Military Specification Mil-M-810F, January 2001, *Environmental Engineering Considerations and Laboratory Tests*
7) HX0032 – *VIRUS Detector System SOW*, Richard Savage
8) HX0033 – *VIRUS Detector System RFP*, Marc Rafal
9) NFPA 79, *Electrical Standard for Electrical Machinery*
10) HX0049 – *VIRUS Spider Assembly*

1.3 Reference Documents

1) IEEE Standard 1100-2005, *Recommended Practice for Powering and Grounding Electronic Equipment (emerald book)*
2) IEEE Standard 142-2005, *Recommended Practice for Grounding of Industrial and Commercial Power Systems (green book)*, Chapter 5, Electronic equipment grounding
3) *Control System Power and Grounding Better Practice*, D. Brown, D. Harrold and R. Hope, Elsevier/Newnes 2004

1.4 Acronyms

See HX0003 − *Acronyms*, for a complete list of HETDEX Project abbreviations and acronyms. A partial list relevant to this document is provided here for the reader's convenience:

AC	**A**lternating **C**urrent
API	**A**pplication **P**rogramming **I**nterface
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
ASME	**A**merican **S**ociety of **M**echanical **E**ngineers
CBA	**C**old **B**lock **A**ssembly
CCD	**C**harge **C**oupled **D**evice
COTS	**C**ommercial **O**ff **t**he **S**helf
CTE	**C**harge **T**ransfer **E**fficiency
ECR	**E**ngineering **C**hange **R**equest
ESD	**E**lectro**s**tatic **D**ischarge
FF	**F**ield **F**lattener

FFLA	**F**ield **F**lattener **L**ens **A**ssembly
FITS	**F**lexible **I**mage **T**ransport **S**ystem
GB	**G**iga **B**yte
GUI	**G**raphical **U**ser **I**nterface
HET	**H**obby-**E**berly **T**elescope
HETDEX	**H**obby-**E**berly **T**elescope **D**ark **E**nergy E**x**periment
IC	**I**nside **C**ryostat
ID	**Id**entification
	Inside **D**ome
IE	**I**nside Spectrograph **E**nclosure
IU	**I**nside **U**pper Electrical Room
LAE	**L**yman-**α** **E**mitter
LN	**L**iquid **N**itrogen
MPP	**M**ulti **P**in **P**hase
MTBF	**M**ean **T**ime **B**etween **F**ailure
MTTR	**M**ean **T**ime **t**o **R**epair
NA	**N**ot **A**pplicable
NFPA	**N**ational **F**ire **P**rotection **A**ssociation
OC	**O**utside **C**ryostat
QE	**Q**uantum **E**fficiency
RFP	**R**equest **f**or **P**roposal
RMS	**R**oot **M**ean **S**quare
RTD	**R**esistance **T**emperature **D**etector
SI	Le **S**ystème **I**nternational d'unités
SOW	**S**tatement **o**f **W**ork
TBD	**T**o **b**e **D**etermined
TBV	**T**o **b**e **V**erified
UPS	**U**ninterruptible **P**ower **S**upply
VDAS	**V**IRUS **D**ata **A**cquisition **S**ystem
VIRUS	**V**isible **I**ntegral-Field **R**eplicable **U**nit **S**pectrograph
VIRUS-P	**VIRUS P**rototype
VIRUS-PP	**VIRUS P**reproduction **P**rototype

1.5 Standards

1.5.1 The International System of Units (SI) shall be used whenever possible.

1.5.2 All drawings shall use metric dimensioning where feasible.

1.5.3 All drawings shall incorporate geometric dimensioning and tolerancing per ASME Y14.5M-1994, *Dimensioning and Tolerancing* or Contractor-proposed international equivalent.

1.5.4 Detector system shall comply with all applicable 2008 National Electric Code standards (NFPA 70 and NFPA 79).

2 Reference Design

2.1 General Description

Experience with VIRUS-P has allowed us to identify technical and scientific risk, and to better understand the trades between material, design, and assembly costs. Although the VIRUS-P detector system has excellent performance, it is not suitable for mass production because it is too expensive and requires too much labor for assembly and testing. A more cost-effective and less labor-intensive design for the VIRUS-PP detector system is described in the remainder of Section 2.

The detector system consists of the following elements that are located inside the spectrograph vacuum cryostats:

- CCD packages
- Vacuum electronics interconnects
- Bulkhead connector

These items are part of the spider assembly which is described in Section 2.2.

Detector system elements that are located outside the spectrograph cryostats include the following items:

- CCD controllers (if not located inside the cryostat as suggested by the left side of Figure 31)
- CCD controller hardware and software interface to the VIRUS Data Acquisition System (VDAS) computer
- Power supplies for the above items (excluding the VDAS computer)
- Electrical and fiber optic interconnects

These items are described in Sections 2.3, 2.4, and 2.5.

Note that some aspects of the design have not been solidified and are subject to modification pending the outcome of ongoing trade studies and Contractor capabilities.

Some pertinent CCD and CCD controller requirements are summarized in Tables 1 and 2. The values in these tables are for reference only. More detailed requirements are presented in the later portions of this document.

Item	Parameter	Value	Requirement
1	Number of Pixels	2064 x 2064	3.1
2	Pixel Size	15 μm x 15 μm	3.1
3	Fill Factor	100%	3.1
4	Image Area	30.72 mm x 30.72 mm	3.1
5	Device Type	Thinned backside illuminated	3.3
6	Quantum Efficiency	≥ 50% (wavelength dependent between 350 nm and 650 nm)	3.5
7	Anti-reflection Coating	Yes	3.7
8	Full Well Capacity	≥ 65,536 electrons	3.8
9	Dark Count	< 1 electron per pixel within a 600 second integration time	3.10
10	Charge Transfer Efficiency	> 0.99999	3.12
11	Readout Noise	≤ 4.2 electrons for any set of CCD and readout electronics	3.5 & 3.18
12	Flatness	Active area surface shall be flat to within ±10 μm with respect to the best fit plane that passes through this surface	4.1
13	Operating Temperature	Between -110°C and -90°C	6.1

Table 1: CCD parameter summary. The values in this table are for reference only. Detailed requirements are given in other sections of this document.

Item	Parameter	Value	Requirement
1	Overscan	32 columns	5.4
2	Integration Period	1.0 to 3600 seconds in 0.1 second increments	5.5
3	Binning (Column x Row)	User selectable 1 x 1 and 2 x 1 (with 1 x 2 and 2 x 2 as a goal)	5.10
4	Number of CCDs	Each controller may service up to 2 CCDs	5.13
5	Controller Crosstalk	$< 10^{-5}$ of the signal	5.14
6	Dynamic Range	16 bits	5.16
7	Linearity	≤ ±1%	3.9 & 5.17
8	Readout Time	≤ 20 seconds for 2 x 1 binning	7.16

Table 2: CCD controller parameter summary. The values in this table are for reference only. Detailed requirements are given in other sections of this document.

2.2 Spider Assembly

Each camera has a spider assembly which consists of the following components as shown in Figure 13:

- CCD package (referred to as the CCD) with integral vacuum electronics interconnect and bulkhead connector (with protective cap as per requirement 10.2)
- FF Lens Assembly (FFLA) with integral focal plane mask and support flexures
- Cold Block Assembly (CBA) with integral heater, temperature sensor, and cold link
- Spider
- Back cap
- Temporary bulkhead connector strain relief (which is only used during the spectrograph assembly process which is described in Reference 7)

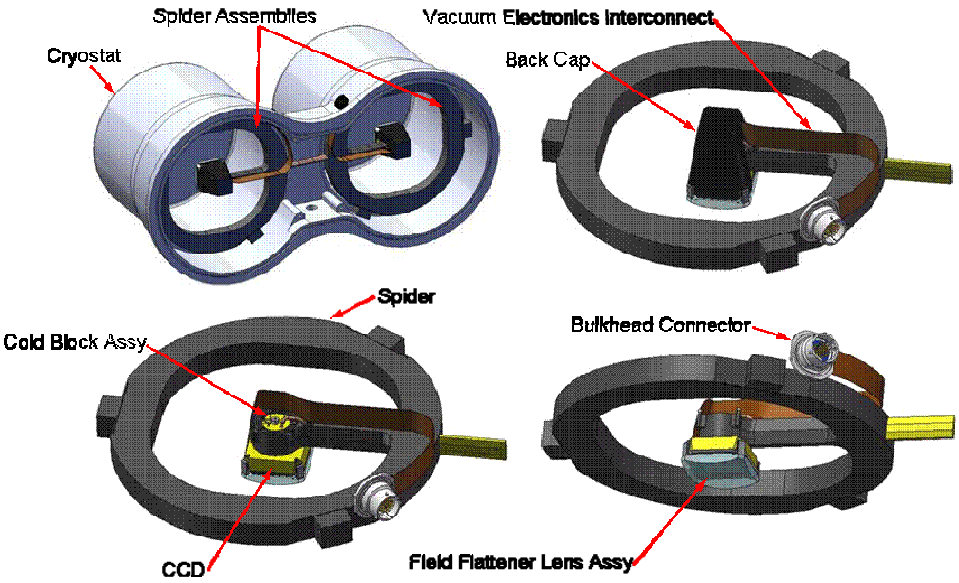

Figure 13: The illustration on the top left is a close up of the cryostat with corrector plates removed to show the location of the spider assemblies. The top right illustration shows the top of a spider assembly with the back cap installed. The two lower illustrations are different views of the spider assembly with the back cap removed.

2.2.1 CCD Package

The CCD package (which will be referred to as the CCD) consists of a silicon sensor die attached to an Invar substrate (Figures 14 and 15). The portion of the silicon die that is light sensitive (i.e., the active area) has 2064 x 2064 pixels that each have a 15 μm square area and 100% fill factor. The CCD is equipped with electronic components as needed (e.g., low noise filters). This includes any auxiliary components and may even include a complete ASIC controller (internal to the vacuum cryostat) as discussed in Section 2.3.

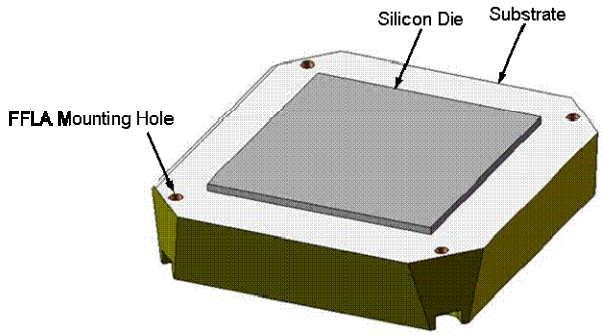

Figure 14: This view of the notional CCD package shows the location of the silicon sensor die and mechanical features (i.e., holes located at each corner of the substrate) used to secure the FFLA to the substrate. Note that the following components are not shown in this figure: vacuum electronics interconnect and auxiliary components.

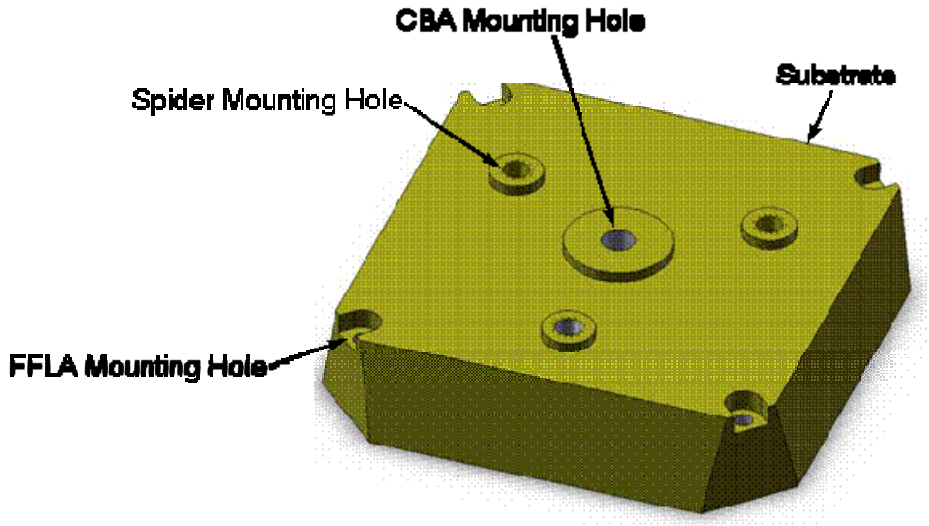

Figure 15: This view of the rear side of the CCD package shows the spider, FFLA, and CBA mounting features. Note that the following components are not shown in this figure: vacuum electronics interconnect and auxiliary components.

2.2.2 Field Flattener Lens Assembly

The FFLA is shown in Figure 16. It is equipped with an integral focal plane mask and four support flexures. The FF lens and focal plane mask are attached to the support flexures via a vacuum-compatible adhesive with low shrinkage and low coefficient of thermal expansion (e.g., Epotek 301-2). The focal plane mask and support flexures are fabricated from Invar and the FF lens is fused silica.

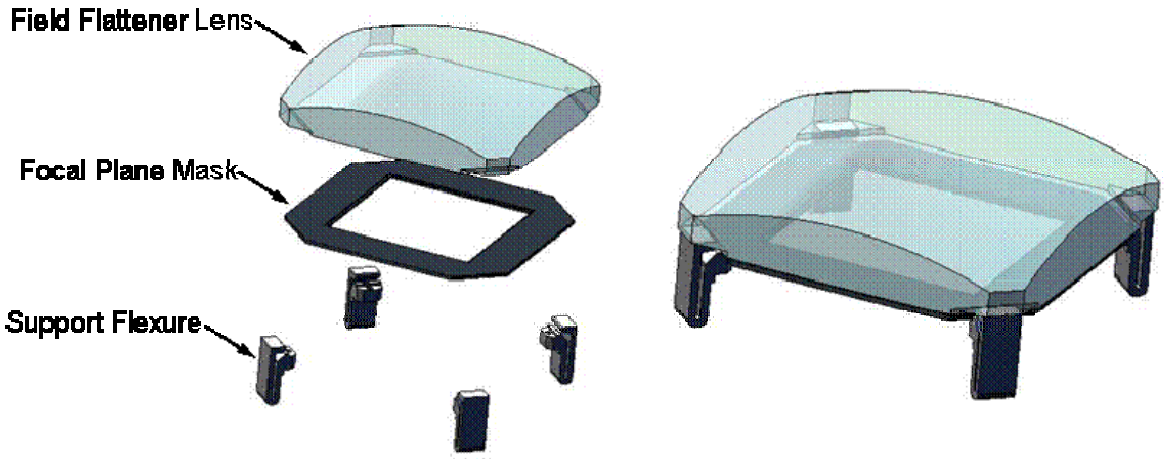

Figure 16: FFLA with FF lens, integral focal plane mask and support flexures. The illustration on the left is an exploded view of the FFLA which is shown in the illustration on the right.

The FFLA is supported by the CCD, and attaches to the top of the CCD via four stainless steel M1.6 screws as shown in Figure 17.

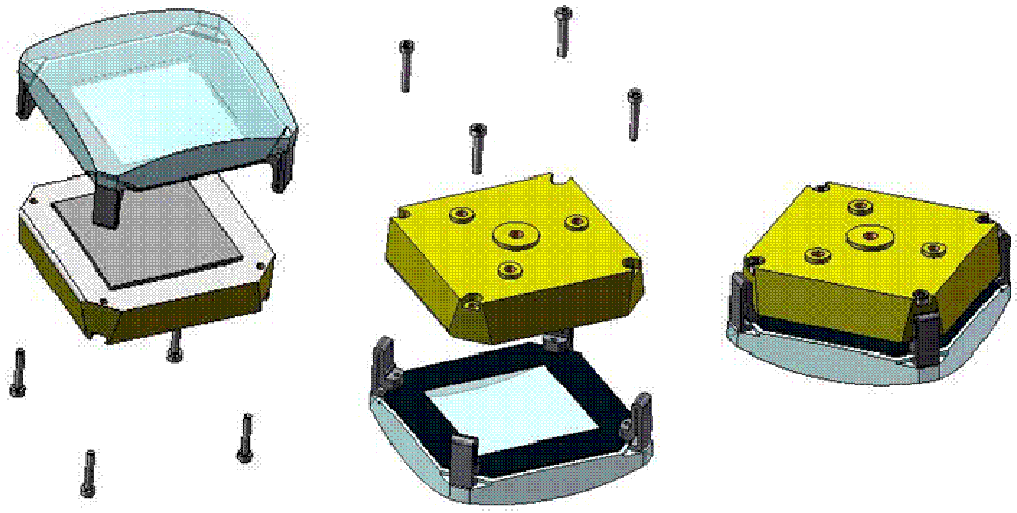

Figure 17: The FFLA attaches to the CCD via four screws.

The alignment between the FFLA and CCD active area is critical and must be maintained at operating temperature to achieve the desired spectrograph optical performance. This can be achieved if the following requirements (see Figures 18 and 19) are met:

1) CCD active area surface is flat, and all points on the CCD active area are within ±10 μm with respect to the best fit plane through this surface.
2) Separation between the rear surface of the FF lens and CCD active area surface is 2500±50 μm
3) Tip and tilt between the FF lens optical axis and the normal to the CCD active area is ≤ 0.03°

4) Centration between the FF lens optical axis and the normal to the center of the CCD active area is within 100 μm of center, and rotation about the optical axis is within ±0.5°.

The first requirement will be met by virtue of the CCD manufacturing process. The second and third requirements will be met as follows:

- The location of the best-fit plane through the CCD active area will be measured with respect to the best-fit plane through the top surface of the CCD substrate
- These measurements will be used when assembling each FFLA to shim the length of each support flexure to achieve the desired separation and tip/tilt when each FFLA is attached to its respective detector package

The fourth requirement will be met by assembling the CCD so that the distance between the center of the CCD active area and CCD substrate flats (i.e., dimensions labeled L in Figure 19) is controlled to within ±50 μm in centration and ±0.5° in rotation.

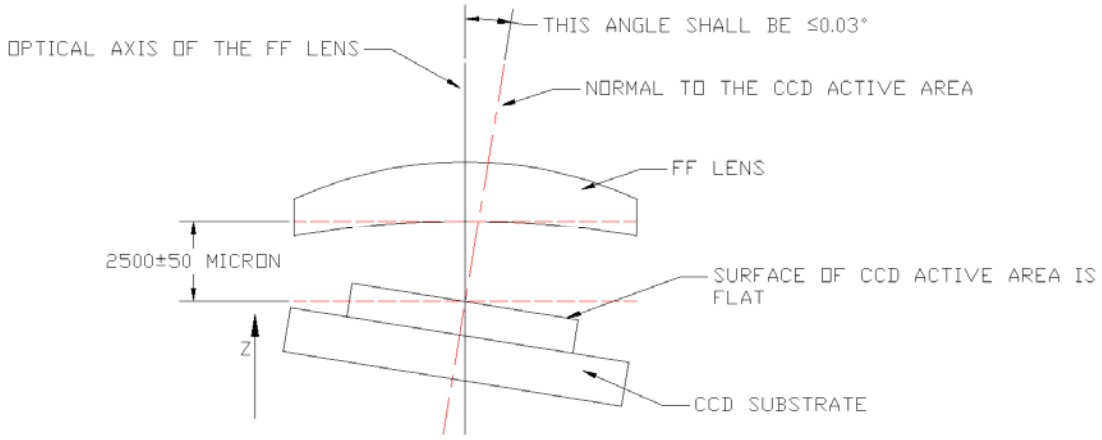

Figure 18: Requirements for the alignment between the FFLA and CCD.

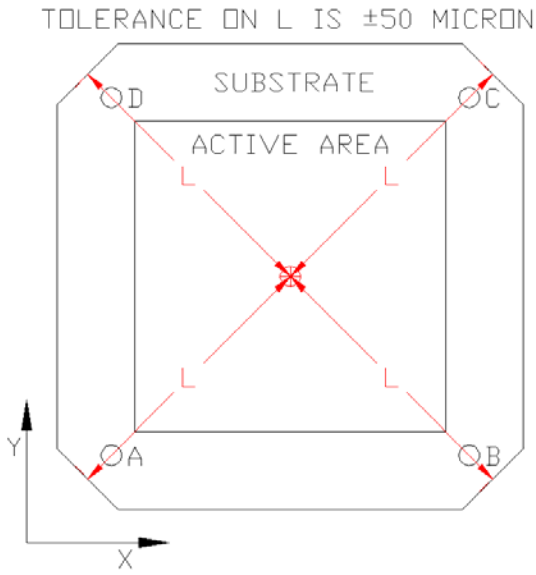

Figure 19: CCD mechanical features used to meet the FFLA/CCD centration and rotation requirements.

2.2.3 Cold Block Assembly

The CBA is shown in Figure 20. It consists of a cylindrical copper piece (referred to as the cold block) that is equipped with an integral heater (e.g., probably four resistors as shown in this figure), temperature sensor (e.g., a glass substrate RTD), and cold link.

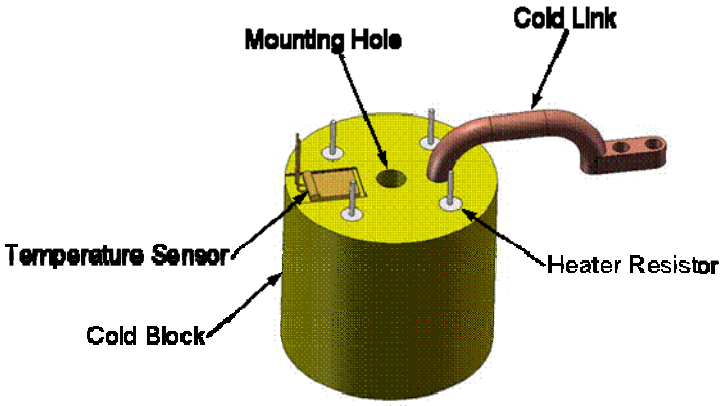

Figure 20: This view of the CBA shows the location of the cold block heater, temperature sensor, and cold link. Note that the cold link is a copper braid and shown schematically in this figure. Also note that the heater resistor pairs are connected in series as shown in Figure 8 and electrically isolated from the cold block.

The CBA attaches to the bottom of the FFLA/CCD assembly via a single vented stainless steel M3 screw as shown in Figure 21.

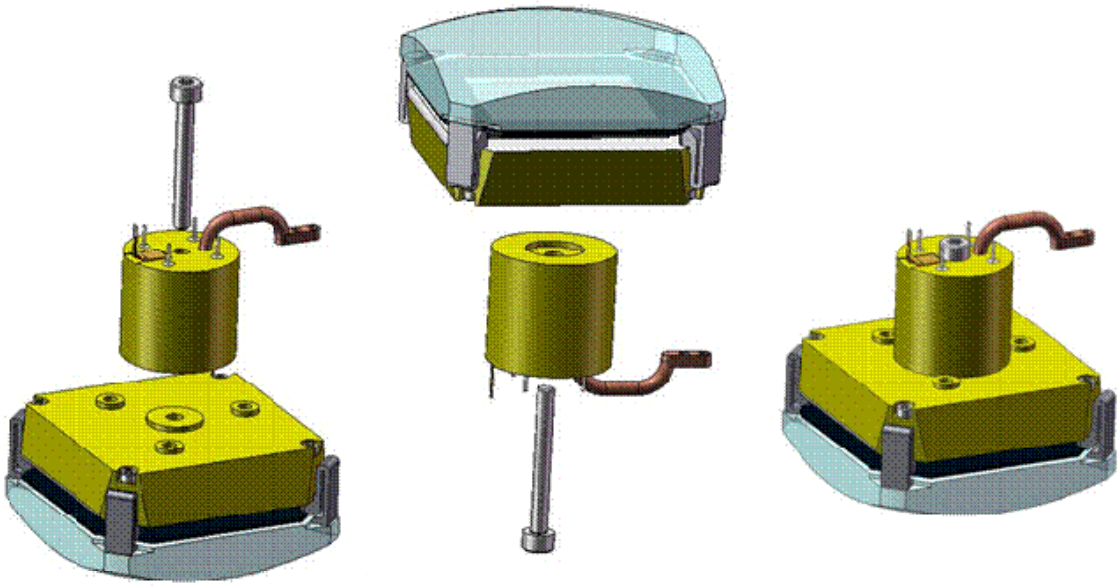

Figure 21: The CBA attaches to the FFLA/CCD assembly via a single screw.

LN removes heat from the CCD via the thermal circuit shown in Figures 22 and 23. A thermally conductive material will be used at the mechanical interfaces between each of these components to enhance the overall conductive heat transfer between the CCD and LN. Note that the thermal resistance of the spider (see Figure 24) and vacuum electronics interconnect are made as large as practical to reduce conductive heat transfer to the CCD from cryostat components that are at ambient temperature.

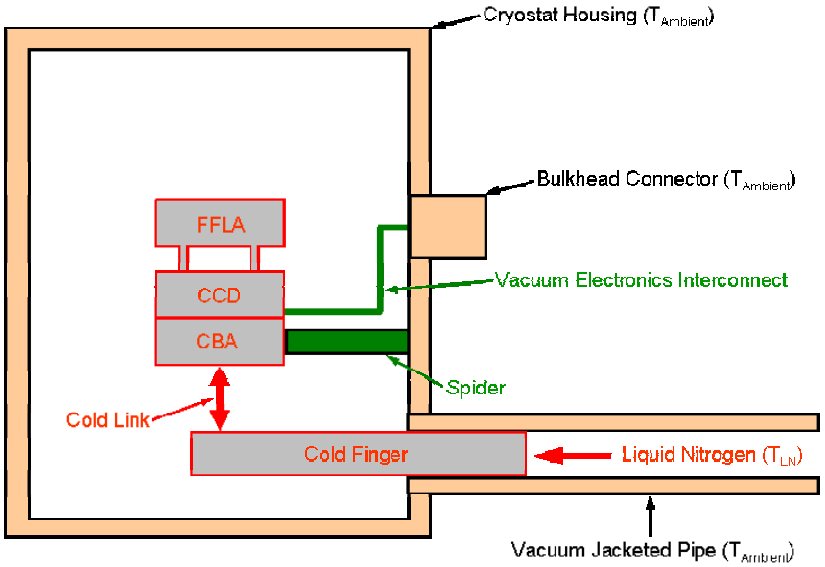

Figure 22: Thermal circuit (illustrated schematically in this figure for a single camera) consists of the following items connected in series: CCD, CBA (with cold link), copper cold finger, and LN. The cold link will be brazed to the CBA. Two M2 copper screws attach the other end of the cold link to the cold finger.

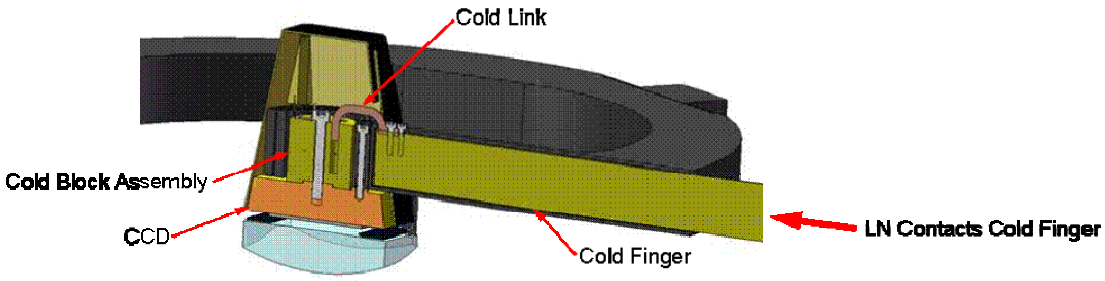

Figure 23: Cutaway view of spider assembly reveals thermal circuit components.

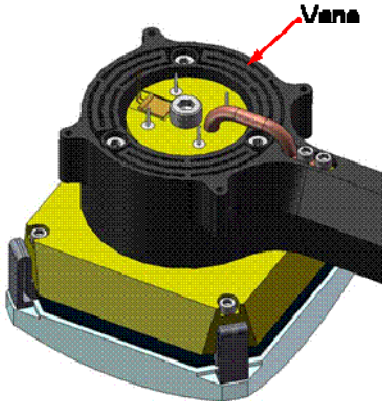

Figure 24: The annular shaped vanes serve to increase the spider's thermal resistance.

To reduce the likelihood of condensate formation on the CCD, the CCD will be maintained at a temperature which is at least 5°C higher than the coldest surface within the cryostat. This (coldest) surface is equipped with a temperature sensor (referred to as cold finger temperature sensor) that is identical to the cold block temperature sensors, and can be monitored to ensure that the CCDs are above this temperature.

Note that each cryostat will be equipped with a vacuum pressure sensor that interfaces to the VDAS computer and is independent of the detector system. As a baseline, we intend to monitor the cold block heater current to sense a vacuum threshold at which the cryostat needs to be re-pumped.

Cold block and cold finger temperature sensors will be used to monitor cryostat cool-down and warm-up rates to ensure that they do not exceed safe limits.

2.2.4 Spider

The spider (Figure 25) is fabricated from Invar. The portion of the spider which protrudes into the optical beam path is referred to as the spider arm.

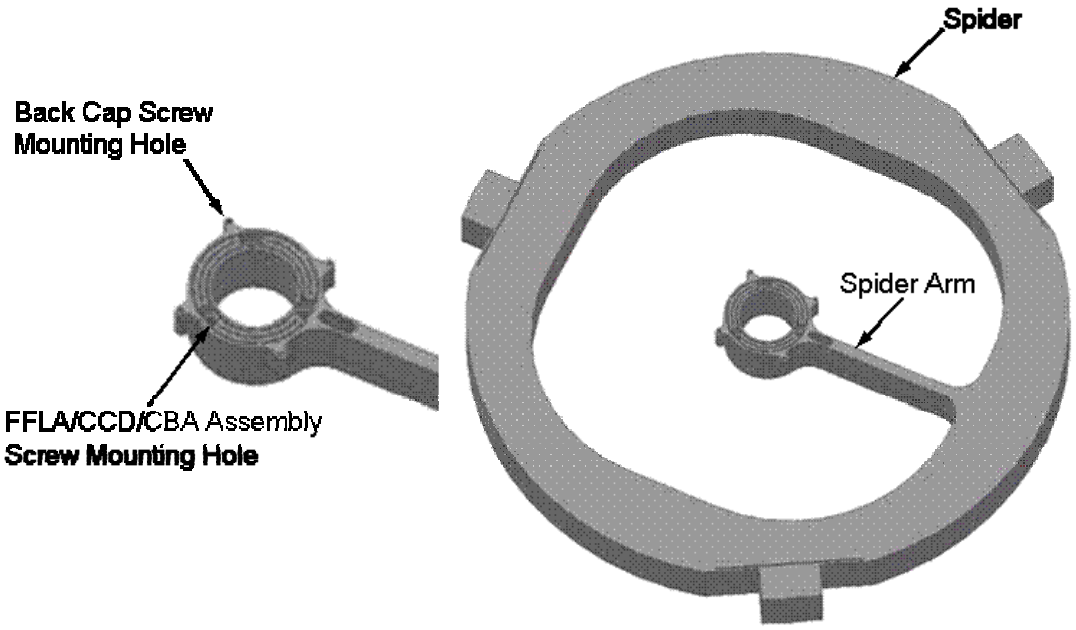

Figure 25: The spider is fabricated from a single piece of Invar.

The FFLA/CCD/CBA assembly attaches to the top of the spider arm via three vented stainless steel M2 screws as shown in Figure 26. After the FFLA/CCD/CBA assembly is attached to the spider, the temporary bulkhead connector strain relief is installed. The strain relief is a simple bracket which secures the bulkhead connector to the spider (to provide protection during the shipping and handling process). This temporary strain relief is removed at the end of the cryostat assembly process just before the spider assembly is mounted inside the cryostat.

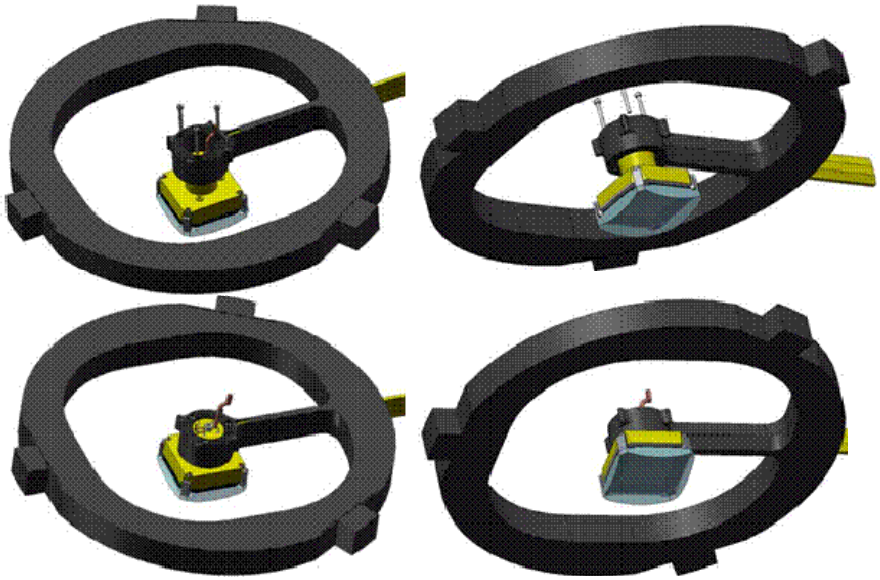

Figure 26: The FFLA/CCD/CBA assembly attaches to the spider via three screws. Note that the vacuum electronics interconnect and bulkhead connector is not shown in this figure.

2.2.5 Vacuum Electronics Interconnect

The vacuum electronics interconnect (Figure 27) interfaces the CCD, cold block heater, cold block temperature sensor, and cold finger temperature sensor to the bulkhead connector. This interconnect is a flex circuit that is equipped with stiffeners and attachment points at appropriate locations. The portion of the interconnect that spans the gap between the CCD and cryostat housing is self-supporting and painted with ALION MH2200 to control stray light (see Section 2.2.9) or equipped with an appropriate cover (see requirement 9.2). The interconnect's conductor length (as measured from the CCD to the bulkhead connector) is approximately 300 mm.

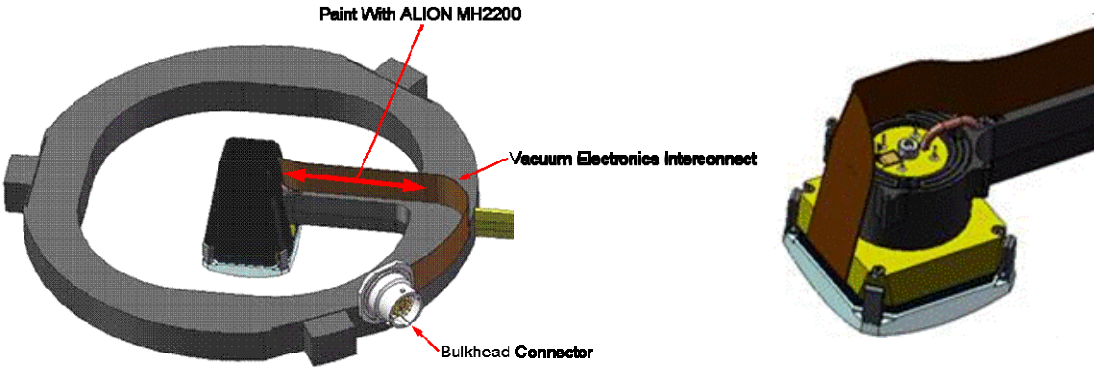

Figure 27: Vacuum electronics interconnect interfaces all electrical components inside the vacuum cryostat to the bulkhead connector. The illustration on the right has the back cap removed to show how the vacuum electronics interconnect is routed to the CCD.

The circuit has multiple layers with ground layers to provide electrical shielding of sensitive signals.

To improve reliability:

- One side of the interconnect is permanently connected via soldered connections to the CCD, cold block heater, cold block temperature sensor, and cold finger temperature sensor
- The other side of the interconnect is permanently connected to the bulkhead connector via soldered connections

Vacuum electronics interconnect thermal resistance is made as large as practical to limit the amount of heat flowing from the bulkhead connector into the cryostat.

2.2.6 Bulkhead Connector

The bulkhead connector is supported by the cryostat housing and is secured to the housing via a jam nut that is located on the outside of the cryostat housing. This allows the spider assembly to be removed from the cryostat housing without disconnecting the bulkhead connector from the vacuum electronics interconnect.

Ideally, the vacuum electronics interconnect would support mounting the bulkhead connectors at the locations shown in Figure 28. Alternative locations can be evaluated as part of the design development.

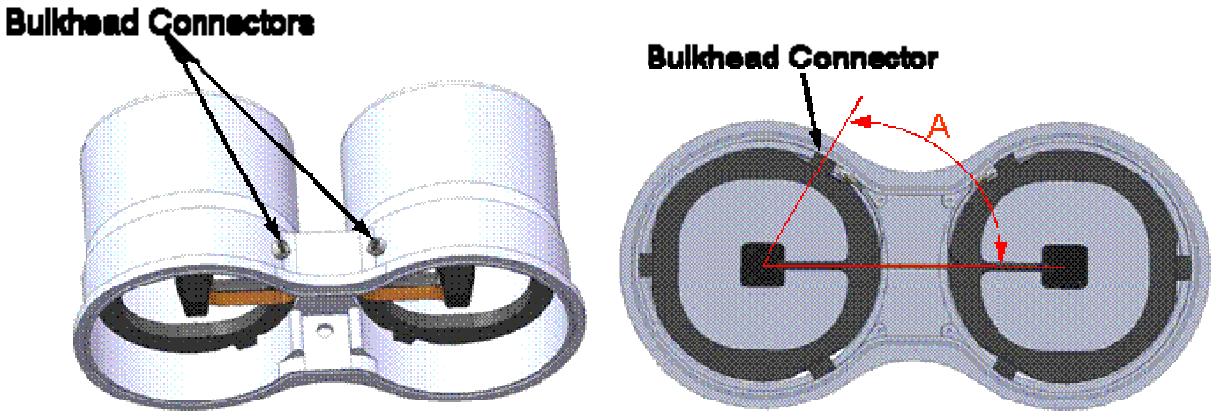

Figure 28: Preferred bulkhead connector location. Angle A would ideally be between 45° and 135°.

The interface between the bulkhead connector and cryostat forms a vacuum seal. Vacuum electronics interconnect conductors are soldered to the pins on the vacuum side of the bulkhead connector. The side of the bulkhead connector that is outside the cryostat is equipped with a male quick disconnect that mates with the CCD controller cable.

2.2.7 Back Cap

The back cap (Figure 29) is used to control stray light (see Section 2.2.9) and is supported by the spider arm. It is secured to the arm via four vented M1.6 stainless steel screws.

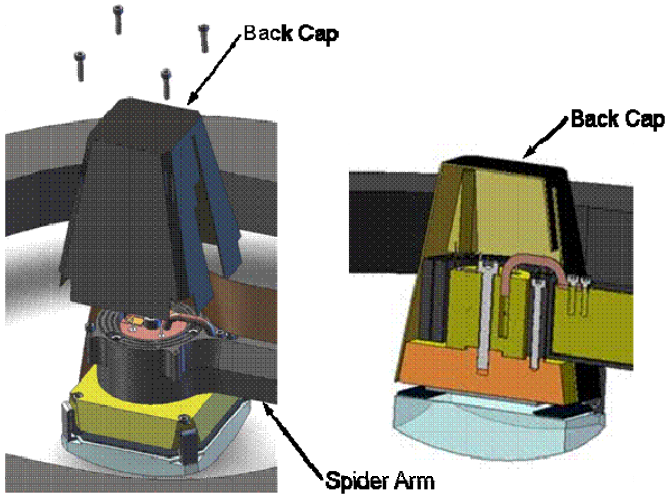

Figure 29: Back cap is secured to the spider via four screws.

2.2.8 Optical Obstructions

Various portions of the spider assembly components (e.g., see spider arm in Figure 30) prevent the light entering the camera from reaching the camera's spherical mirror. The spider assembly components are designed to minimize this obstruction. In general the:

- Bulkhead connector does not protrude into the optical path and cause an obstruction
- Vacuum electronics interconnect is mounted so that it lies within the obstruction of the spider arm
- CCD is within the shadow of the obstruction caused by the back cap

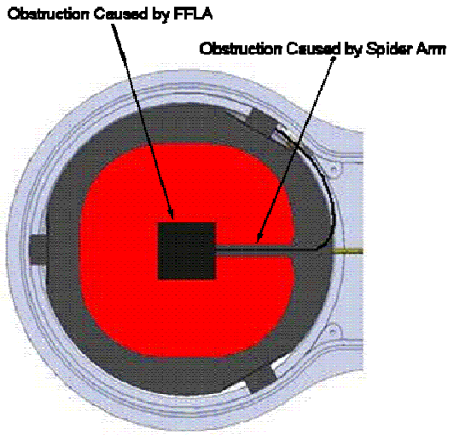

Figure 30: View as seen looking into the spectrograph. The area highlighted in red represents the portion of the optical path which is not obstructed by the spider assembly.

2.2.9 Stray Light

Spider assembly component surfaces (excluding the FF lens and CCD light sensitive area) which are exposed directly to primary optical beam or indirectly to stray light, are painted with ALION MH2200 to control stray light. ALION MH2200 is a black optical thermal control coating (containing organic silicon) that is manufactured by ALION Science and Technology Corporation. It is a vacuum compatible flat black optical absorber coating used in telescopes and other equipment in which light scattering is an issue. All parts painted with ALION MH2200 are vacuum baked for four hours at 150°C to cure the paint and remove xylene-based contaminants which would otherwise degrade the cryostat vacuum and put the CCD in risk of contamination.

2.2.10 Radiative Heat Transfer

Gold coatings are used where appropriate to limit radiative heat transfer to the CCD, cold block, thermal link, and cold finger. The current plan assumes that the following components will be gold plated:

- Inside of the cap
- Cold finger
- Cold block

2.3 Detector System Architecture

The detector system has 192 CCDs that interface to HET's VDAS computer. Several different detector system architectures can be envisioned at this time. The final system architecture depends upon the capability of the Contractor selected to provide the detector system, and the architecture's ability to meet all of the relevant requirements contained in this specification.

For example, each spectrograph pair can be serviced by one or two controllers as shown in Figure 31. In the first case (left side of Figure 31) each CCD has a dedicated ASIC controller that is located inside the vacuum cryostat. In the second case (right side of Figure 31) a single controller located outside the vacuum cryostat services two CCDs. This concept has the advantage that the controller can be easily replaced without opening the vacuum cryostat (a delicate, time-consuming procedure). However, this concept has the disadvantage that it increases the length of the signal cables.

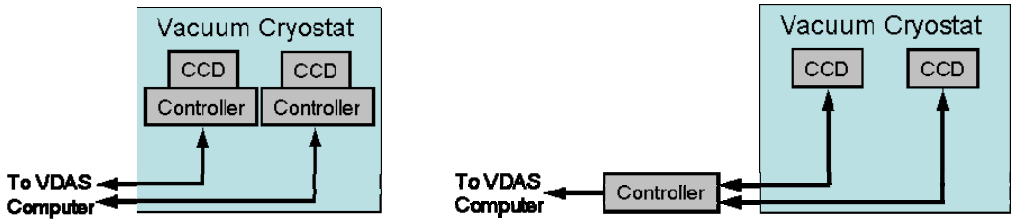

Figure 31: Possible cryostat CCD and controller arrangements.

The controllers can communicate directly to the VDAS computer, or to the VDAS computer through one or more multiplexers (or auxiliary controllers). The left side of Figure 32 depicts the spectrographs in each of the two enclosures communicating with the VDAS computer via two multiplexers, one associated with each enclosure. The right side of Figure 32 depicts each column of spectrographs communicating with the VDAS computer via a multiplexer.

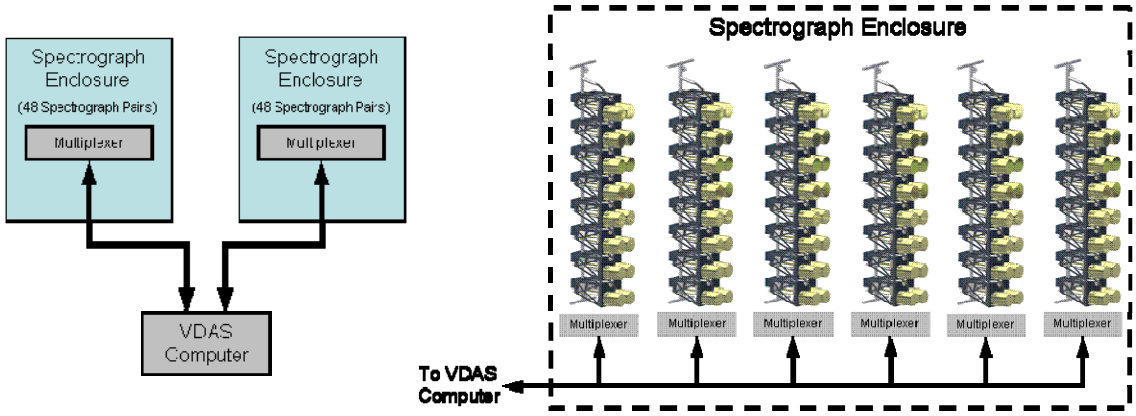

Figure 32: One or more multiplexers may be used to interface the CCD controllers to the VDAS computer.

Experience with the McDonald Observatory Version 2 CCD controller (as well as other controllers) indicates that special precautions must be taken to reduce crosstalk, especially when multiple CCDs and controllers are operating in close proximity to one another in a single large electronics enclosure (i.e., the spectrograph enclosures). In particular, this experience suggests that when reading out all of the CCDs, it is desirable to have the clock pulses closely synchronized to ensure that the charge is moved between the "CCD charge buckets" as simultaneously as possible. This could be accomplished by using a single master clock sequence generator to feed all of the CCD controllers simultaneously, or by triggering the read sequence simultaneously in all controllers from a common clock pulse.

2.4 VIRUS Data Acquisition System Computer and Interface

The VDAS computer is a rack-mounted PC that is running Red Hat Enterprise Linux 5. The baseline computer is a Dell PowerEdge 2950 III. At a minimum it is equipped with dual 3 GHz class CPUs, 4 GB of RAM, redundant power supplies, two or more PCIe slots, with at least 500-GB of mirrored disk storage.

Ideally the VDAS computer would be located in the upper electrical room which is located one floor below the base of the telescope. If this is not possible (e.g., due to a control line length restriction), it could be located in one of the spectrograph enclosures (shown in Figure 12), or possibly in another enclosure located elsewhere on the telescope.

If the VDAS computer is located in the upper electrical room, any interconnect cable between the VDAS computer and a spectrograph enclosure needs to be at least 55 m long to accommodate various physical constraints (which includes the cable wrap described in Section 2.7).

The detector system computer interface resides in the VDAS computer and connects to the remainder of the detector system via fiber optic cable. This computer interface would ideally be a COTS PCIe interface card, using Ethernet or other mutually agreed-upon communications protocol. If Ethernet is used, multiple ports could be provided on one or more PCIe interface cards.

2.5 Power Supplies

The power supplies supply electrical power to the detector system. The number of power supplies and their locations have not been determined yet. One concept is illustrated in Figure 33. In this concept there are 12 power supplies; six rack-mounted inside each spectrograph enclosure, each servicing a column of 16 spectrographs (i.e., eight spectrograph pairs). Note that one or more power supplies can be located in the upper electrical room. This has the advantage that it reduces the amount of heat generated in the dome which can adversely affect the telescope's image quality. However, it requires longer cable lengths and more space in the cable wrap (see Section 2.7).

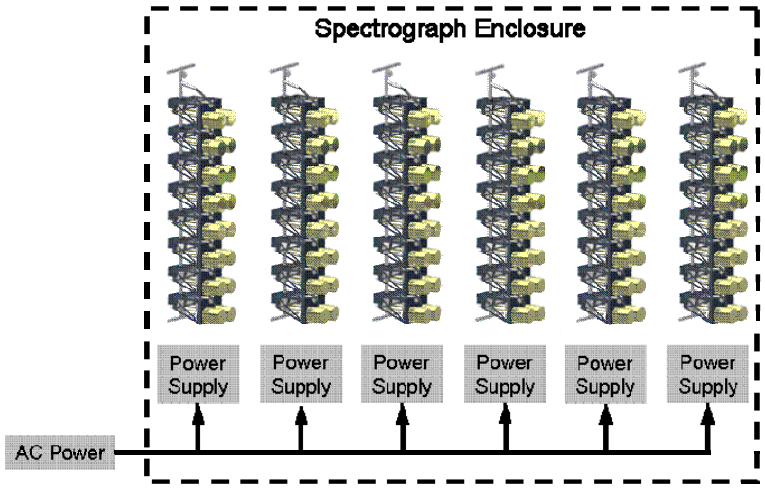

Figure 33: Each power supply services eight spectrograph pairs.

The detector system power supplies will be equipped with over-current, over-voltage, and under-voltage monitors. The VDAS computer will use the monitor signals to ensure the safety of the CCDs.

A standby UPS will provide AC power (at 90 to 130 VAC, 60±5 hz), via a 3-wire system (with hot, neutral and ground wires) to the detector system power supplies. The UPS will have sufficient backup capacity (approximately 10 to 15 minutes) to allow the observatory backup generator to automatically come on-line in the event of a grid power failure. The intention is that the spectrographs shall operate continuously throughout a power outage as the facility transitions from line power to generators and back.

The standby UPS will provide AC power at three locations:
- Upper electrical room equipment rack
- Each of the spectrograph enclosures

Detector system connection to the AC power at each location is through three terminal blocks that are equipped with safety covers.

Detector system electrical power control will be via a single start/stop latching relay circuit. The circuit will have two momentary push buttons referred to as the Start and Stop buttons. When the Start button is momentarily depressed, AC power is automatically applied to the entire detector system. When the Stop button is momentarily depressed, AC power is automatically disconnected from the entire detector system. The latching relay is used to ensure that someone has to physically restart the system after there has been a loss of electrical power. The Start and Stop buttons would be located in the upper electrical room.

2.6 Spectrograph Enclosures

Two spectrograph enclosures are located at the base of the telescope as shown in Figure 12. The enclosures are approximately 4.9 m wide by 1.3 m deep by 3.8 m tall. The spectrographs are arranged upon a rectangular grid within each enclosure in a fixed position with respect to gravity.

The spectrographs are inserted into the enclosure slots from the front. Each slot has a unique address that can be read by the detector system. The hardware which encodes each address is referred to as an address generator. The address generator and reader hardware could consist of a configuration of eight magnets that are sensed by magnetic reed switches, eight cams and limit switches, or more simply by a 9-pin cable and connector that has signal pins connected to the ground pin.

Additional room is provided in the bottom of each enclosure for ancillary detector system equipment (e.g., detector system power supplies and auxiliary controllers). The additional room in each enclosure is approximately equivalent to eight 19" wide by 10U (i.e., 17.5") high equipment racks that are located side by side. The depth of each rack will be limited to a maximum of 23.88" (i.e., 606 mm).

All items in the enclosure are only accessible from the front of the enclosure, and will be rack mounted on slides as appropriate.

The enclosures will be electrically grounded and shielded, light tight, thermally insulated, environmentally sealed, and positively pressurized. They will be:

- Continuously purged with dry filtered air to prevent ingress of dust and moisture, especially when the enclosure doors are open to facilitate scheduled and unscheduled maintenance activities
- Actively controlled as necessary with sufficient air flow to maintain the detector system components (which reside inside the enclosure) within their specified operating temperature and humidity ranges.

Each enclosure will also be equipped with automatic thermal shutoffs (i.e., under and over temperature) that provide a signal which can initiate the safe and orderly shutdown of all items within the enclosures (including the detector system electronics). The reference design assumes that:

- This signal is used to automatically disconnect electrical power from the enclosures
- Each item inside the enclosures can automatically and safely shutdown when power is terminated without prior warning.

2.7 Telescope Cable Wrap

The base of the telescope is attached to a pintle bearing which allows the entire structure to rotate (in azimuth at a maximum rate of 4.0 deg/sec) about a vertical shaft that is anchored in the concrete floor. The cable management system, referred to as the "cable

wrap" (see Figure 34), is located at the base of the telescope and allows cables going to the rotating telescope structure to handle up to 540° of rotation. All detector system cables (which are external to the vacuum cryostats) that run between the spectrograph enclosures and upper electrical room will pass through the cable wrap.

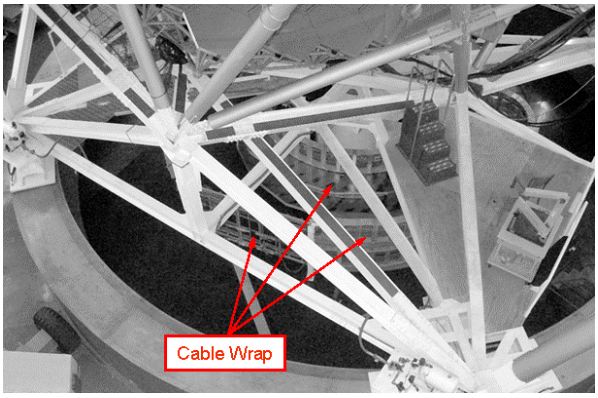

Figure 34: Telescope cable wrap winds and unwinds (like a clock spring) as the telescope rotates in azimuth by as much as 390°. The length of the flexible portion of the cable wrap is approximately 20 m.

2.8 Optical Shutter

The optical fibers feeding the spectrographs receive light at the telescope's focal surface. An optical shutter located just below the focal surface is used to control light feeding these fibers. During an observation of the sky (referred to as an exposure), the shutter must be open while the CCDs are integrating (i.e., acquiring data). Additionally, during the CCD readout period the shutter must be closed. A common time base is used to ensure that the shutter and CCDs are properly synchronized.

The period of time that the shutter is open is referred to as the exposure period. The period of time that the CCDs are acquiring data is referred to as the integration period. The temporal relation between these two periods is shown in Figure 35. Note that, because the shutter employs a rotary mechanism, the time to transition the shutter between its "open" and "closed" positions is on the order of one second and is symmetric, so that all spectrographs see the same total exposure period.

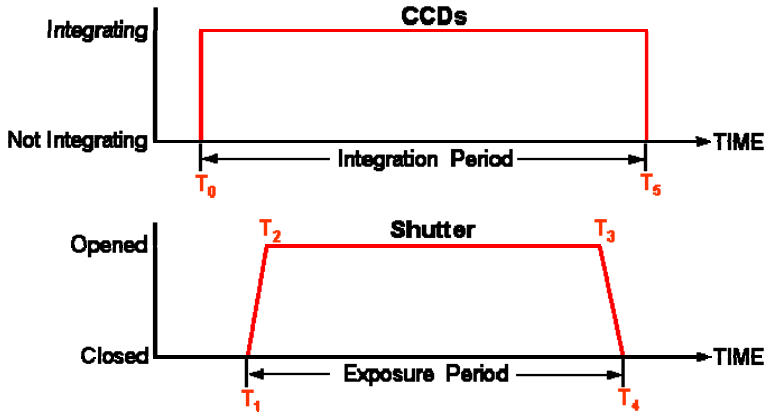

Figure 35: This schematic diagram illustrates the temporal relationship between the shutter exposure period and the CCD integration period. Note that $T_0 < T_1 < T_2 < T_3 < T_4 < T_5$.

The VDAS computer controls the shutter and the detector system (i.e., the shutter and detector system do not communicate directly with one another). Prior to conducting an observation (i.e., an exposure), the VDAS computer sends the shutter the length of the desired exposure period. It also sends the detector system the desired length of the integration period. Note that the exposure period is always less than the integration period. After these parameters are received by the shutter and detector system, the VDAS computer initiates an exposure by sending the shutter and detector system each a Perform Light Exposure command. This command includes a Start Time parameter, which tells the shutter and detector system when the observation is to begin. The start time is given in hours, minutes, and seconds (in the universal time system), and has the same value for both the shutter and detector system. Note that the shutter controller has a (user-adjustable) delay parameter that ensures the shutter opens after the detector system has started integrating.

Just before the Start Time (at T_0 in Figure 35) approaches, the detector system automatically flushes the CCDs. The "flushing" is timed so that the flushing is completed by T_0. After the integration period has been completed (at T_5 in Figure 35), the detector system automatically reads out the CCD and transmits the data to the VDAS computer system.

2.9 Operational and Support Concept

The detector system operates 365 nights per year, except during planned shutdowns. To maintain detector system stability the detector system components are:

- Powered continuously
- Items inside the vacuum cryostat will be maintained within their specified operating temperature range.

Planned detector system shutdowns will occur no more frequently than once every six months. During the shutdowns the electrical power and cryostat cryogenic cooling may be shut off for periods of up to two weeks.

If a non-catastrophic detector system failure or problem occurs at night, it will not be diagnosed and fixed until the following morning. A goal is to design the system so that the telescope operator can (without leaving the control room) quickly identify and isolate the failed/problem components (via software control) so that he can continue operating the detector system at reduced capacity. Another goal is to design the system so that the following morning the failure/problem can be easily diagnosed and repairs completed within a four-hour period. This four-hour period assumes:

- Failures are only traced down to the field-replaceable module level
- Components inside the vacuum cryostats do not have to be replaced
- An adequate supply of field-replaceable spares is on site.

If components inside the vacuum cryostats need to be replaced/repaired the affected camera pair will be removed from the spectrograph enclosures and then repaired in a clean-room environment.

3 CCD Requirements

3.1 CCDs shall have 2064 x 2064 pixels in the active image area, with 15 μm x 15 μm pixels, and a 100% fill factor.

3.2 CCD Modulation Transfer Function (MTF) shall be ≥ 25% at the Nyquist frequency (which is 33 line pairs/mm). Compliance shall be verified by modeling.

3.3 CCDs shall be thinned and back-illuminated for enhanced UV and blue response.

3.4 Requirements 3.5, 3.6, 3.9, 3.10, 3.11, 3.12, 3.13, 3.14, 3.15, 3.16, and 3.18 shall all be met over the operating temperature range specified in requirement 6.1.

3.5 The CCD Quantum Efficiency (QE) of the pixels in the active area of each CCD (excluding non-functional pixels as defined in requirement 3.15) shall have QE greater than the minimum QE that is shown in Table 3.

Wavelength (nm)	Minimum QE
350	50%
375	60%
400	70%
500	75%
650	65%

Table 3: Minimum acceptable QE as a function of wavelength for individual CCDs.

Additionally, the median QE of a cumulative batch of CCDs shall have QE equal to or greater than the values given in Table 4 (and Figure 36) as a function of wavelength and system median read noise.

Wavelength (nm)	System Median Read Noise for a Cumulative Batch (electron)			
	2.5	**3.0**	**3.5**	**4.0**
350	50%	55%	61%	67%
375	66%	70%	75%	79%
400	77%	80%	84%	88%
500	78%	80%	83%	85%
650	68%	70%	72%	75%

Table 4: Minimum acceptable median QE as a function of wavelength and system median read noise for a cumulative batch of CCDs. See 3.18 and 5.11 for the read noise requirement.

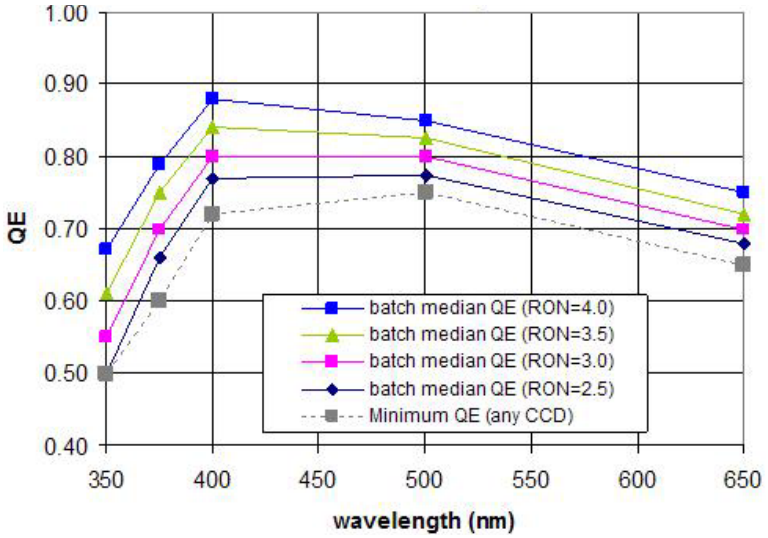

Figure 36: Minimum acceptable QE for any CCD and cumulative batch of CCDs.

Note that the concept of a "cumulative batch of CCDs" referred to in 3.5 (as well as in requirements 3.16 and 3.18) shall be interpreted as follows.

- During the first production run (see HX0032 Section 8), 16 CCDs shall be delivered. Therefore, for the first production run the batch is the 16 CCDs.
- During the second production run an additional 48 CCDs shall be delivered. However, the batch shall consist of all the CCDs delivered during the first and second production runs.
- During the third production run an additional 86 CCDs shall be delivered. However, the batch shall consist of all the CCDs delivered during the first, second and third production runs.
- During the (optional) fourth production run an additional 50 CCDs shall be delivered. However, the batch shall consist of all the CCDs delivered during the first, second, third, and fourth production runs.

3.6 QE uniformity at any single wavelength between 350 nm and 650 nm, of the functional pixels within a single CCD, shall be within ±10% of the CCD's mean QE at that wavelength.

3.7 The CCD active area surface shall have an anti-reflection coating that is optimized for the 350 nm to 550 nm wavelength range. This anti-reflection coating shall not be graded. Light in the 350 nm to 550 nm range is incident upon the CCD at a range of angles, some of which are as high as 42°. The anti-reflection coating shall be optimized for an incident angle of 15° and verified for the maximum angle of incidence.

3.8 Minimum CCD full well capacity shall be in excess of 65,536 electrons and shall be sized to meet the linearity requirement 3.9.

3.9 The combined response of the CCD and controller shall be linear to $\leq \pm 1\%$ over the entire 16-bit dynamic range (see requirements 5.17 and 5.16). Linearity shall be measured via a mutually agreed-upon technique, and corrections necessary to remove response nonlinearity shall be provided in a mutually agreed upon format (e.g. lookup table, etc). The final corrected combined response of the CCD and controller shall be linear as follows:

- Better than ±0.5% over the entire 16-bit dynamic range (see requirements 5.17 and 5.16)
- Better than ±0.1% over the first 10% of the 16-bit dynamic range.

Since we do not anticipate recalibrating the CCD linearity on a regular basis the linearity calibration must be stable over a long period of time (preferably greater than two years).

3.10 CCD dark count shall be < 1 electron per pixel within a 600 second integration time.

3.11 CCD dark signal uniformity shall be ±0.2 electrons peak-to-peak in 600 seconds.

3.12 Both serial and parallel Charge Transfer Efficiency (CTE) per pixel shall be better than 0.99999 as measured at a signal level of 2000 electrons (or lower) with a mutually agreed-upon technique.

3.13 Residual charge images following exposure to bright objects up to half full well capacity shall be less than 2×10^{-5} times the bright object signal, as measured with a mutually agreed-upon technique.

3.14 The residual charge resulting from exposure to bright objects over half full well capacity shall not exceed 1/300 electrons per second after 20 minutes of exposure. If required, the Contractor shall provide some means to minimize the residual charge image. For example, the CCD controller could have the ability to simultaneously flush some of the CCDs (i.e. the ones that have been exposed to bright objects) to minimize the residual image while all of the other CCDs are acquiring data (see requirement 7.18).

3.15 Fewer than 0.2% of the pixels on each CCD chip shall be non-functional (defined as blocked, a trap, a hot pixel [i.e. a pixel with greater than 0.5 electrons/sec], or a dark [< 80% of mean QE] pixel).

Note that a trap is defined as a pixel that temporally traps a charge of 25 electrons or greater. The test to identify such traps shall involve taking low and high level flat field exposures and then taking their ratio as described by the formula below. Specifically, the median of ten frames exposed at the 250 electron level (with flushes between each to empty traps), will be divided by the median of three frames exposed at the 50,000 electron level (with flushes between each to empty traps), and a trap will be defined as any pixel satisfying the following relation:

$$\frac{200 \cdot \text{LowLevelFlat}}{\text{HighLevelFlat}} < 0.9$$

3.16 The number of nonfunctional columns (i.e. hot columns and blocked columns) and traps shall conform to the requirements stipulated in Table 5.

	Nonfunctional Columns	Traps
Median for a cumulative batch of CCDs	Fewer than 1.5	≤ 20
Maximum for a single CCD	3	≤ 40

Table 5: CCD trap, hot and blocked column requirements.

3.17 CCD shall be capable of user selectable binning of 1 x 1 and 2 x 1 (columns x rows). As a goal, CCD shall also be capable of user selectable binning of 1 x 2 and 2 x 2 (columns x rows).

3.18 The maximum system read noise for any set of CCD and readout electronics shall be 4.2 electrons for all binning modes and readout times.

3.19 Each CCD shall have two pairs of two on-chip amplifiers, and:

- Each CCD shall be configured at the factory to use the best pair. When configured to use two amplifiers, amplifier #1 shall read rows 1 through 1032 and amplifier #2 shall read rows 1033 through 2064. It shall also be possible to use jumpers to switch to another pair of amplifiers if one of the amplifiers in the first pair fails (note that when pairs are switched out it will be necessary to change the CCD readout order).
- As a goal, each CCD shall be able to be configured (through jumpers) so that it can be read out through any one of its four amplifiers. Additionally, as a goal, when the system is configured to use one amplifier, it shall be possible to read out each CCD at twice the rate that it would be reading out if two amplifiers were being used.
- As a goal it shall be possible to change the jumpers (mentioned in the previous two bullets) in a clean room enviornment without soldering; provided performance/reliability is not compromised.

3.20 The electrical interface between the CCD and CCD controller shall be as per requirement 5.19.

3.21 As a goal, the vacuum electronics interconnect shall attach to the CCDs as indicated in Figure 37.

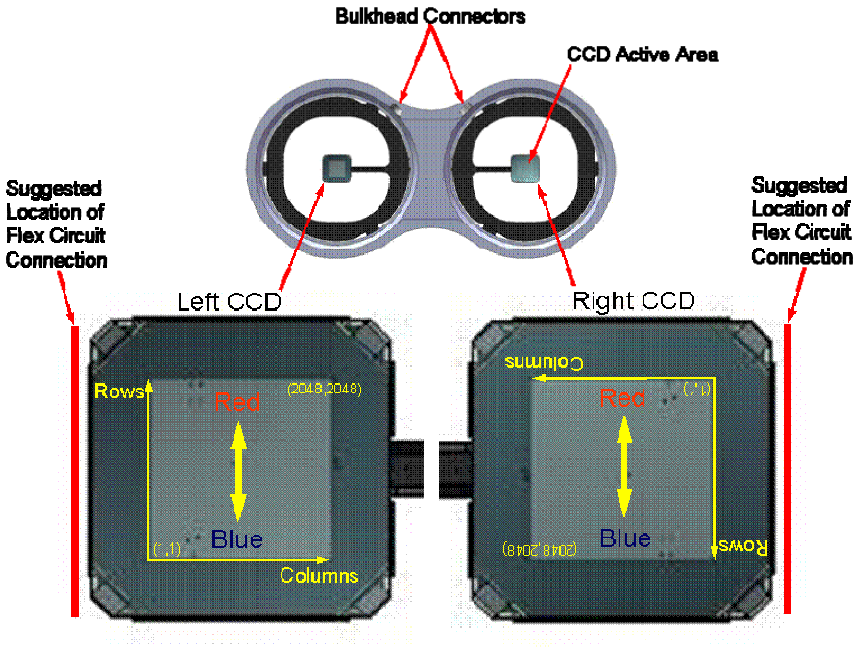

Figure 37: The top illustration is a view looking towards the camera FF lens and CCD active area. The bottom illustrations are close up views of the left and right CCDs and show that the spectral direction is along rows (i.e., up and down, as shown in this figure) and the spatial direction is along columns (i.e., left and right, as shown in this figure). The light is dispersed along the column direction with the blue and red portions of the spectrum oriented as indicated by the Blue and Red labels (that are associated with the vertical yellow line that is truncated by arrows on each end).

3.22 CCD substrate shall be Invar.

3.23 CCD shall utilize Multi Pin Phase (MPP) technology to improve performance.

3.24 Summing well capacity shall be twice the capacity of the serial register, and the serial register capacity shall be twice the CCD full well capacity.

4 FFLA, CBA, Back Cap, and Spider Interface Requirements

4.1 At operating temperature, the CCD active area surface shall be flat (see Figure 18) to within ±10 µm. This shall be verified by:

1) Measuring the location of at least 25 points that lie on the active surface where:
   - The points shall be spaced on a square grid whose sides are approximately 95% of the width of the CCD active area
   - The Cartesian coordinates of each point shall be measured with an accuracy of 100 µm in X and Y, and 2 µm in Z
   - Z shall be normal to the top surface of the CCD substrate and orthogonal to X and Y

2) Fitting a best-fit plane through the measured points
3) Showing that all of the measured points are within 10 μm of the best-fit plane surface

4.2 At operating temperature, the top surface of the CCD substrate shall be flat to within ±10 μm. This requirement only applies to the portions of the substrate surface that will be in direct contact with the FFLA support flexures (i.e., in the vicinity of A, B, C, and D in Figure 19).

This shall be verified by:
1) Measuring the location of 12 points that lie on the CCD substrate where (see Figure 19):
   - 3 points shall be in the vicinity of A
   - 3 points shall be in the vicinity of B
   - 3 points shall be in the vicinity of C
   - 3 points shall be in the vicinity of D
   - The Cartesian coordinates of each point shall be measured with an accuracy of 100 μm in X and Y, and 2 μm in Z
   - Z shall be normal to the top surface of the CCD substrate and orthogonal to X and Y
   - These measurements shall be made with the same setup that was used to make the measurements associated with requirement 4.1
2) Fitting a best-fit plane through the measured points
3) Showing that all of the measured points are within 10 μm of the best-fit plane

4.3 CCDs shall be equipped with mutually agreed-upon FFLA mechanical interface. This interface shall be compatible with the mutually agreed-upon procedure for assembling the FFLA/CCD assemblies so that the following requirements can be met at operating temperature:
- Separation between the rear surface of the FF lens and CCD active area surface shall be 2500±50 μm (see Figure 18)
- Tip and tilt between the FF lens optical axis and the normal to the CCD active area (defined as the normal to the plane or vertex of the sphere at the center of the detector active area) is ≤ 0.03° (see Figure 18)
- Centration between the FF lens optical axis and the normal to the center of the CCD active area is within 100 μm of center (see Figure 19), and rotation about the optical axis is within ±0.5°.

4.4 CCDs shall be equipped with mutually agreed-upon mechanical CBA interface. This interface shall include features which control the angular orientation of the CBA with respect to the CCD substrate (e.g., a pin in the CBA which mates with a slot in the back of the CCD substrate) to within ±2.0°.

4.5 The interface between the CCD and CBA shall be prepared following best practices to ensure a good thermally conductive connection between the CCD and

CBA, and shall have mechanical features that accurately locate/orient these items with respect to one another so that at operating temperature:

- Tip and tilt between the CBA cylindrical axis and the normal to the back surface of the CCD package shall be ≤ 0.5°
- Centration between the CBA cylindrical axis and the normal to the CCD active area shall be within 0.5 mm of center.

4.6 Back cap shall be equipped with mutually agreed-upon mechanical features to accommodate the routing of the vacuum electronics interconnect.

4.7 The interface between the CCD and spider shall have mechanical features that accurately locate/orient these items with respect to one another so that at operating temperature, and at temperatures between 18°C and 32°C:

- Tip and tilt between the spider central axis and normal to the CCD active area shall be ≤ 0.2°
- Centration between the spider central axis and normal to the CCD active area shall be within 0.25 mm of center, and rotation about the central axis is within ±0.5°

4.8 Spider assembly shall be equipped with mutually agreed-upon mechanical interfaces for securing the vacuum electronics interconnect.

4.9 CCDs shall be oriented in the spectrograph cameras so that dispersion is along rows and the spatial direction is along columns (as shown in Figure 37).

4.10 Note that for requirements 4.3, 4.4, 4.5, 4.6, 4.7, and 4.8:

- The University is responsible for integrating the CCDs with the other spider assembly components and achieving the final alignment between the CCDs and remainder of the spider assembly and cryostat components
- After the mechanical interfaces between the CCDs and other spider assembly components is mutually agreed upon, the Contractor is only responsible for manufacturing their CCDs to the mutually agreed upon dimensions and mechanical tolerances, and are not responsible for the dimensions and mechanical tolerances of the other spider assembly components that are supplied by the University

5 CCD Controller Requirements

5.1 Controllers shall be able to flush (i.e., clock CCDs and dump the charge without digitizing the data and without sending it to the VDAS computer system) all CCDs in a time period which is consistent with requirement 7.16.

5.2 A shutter is used to control the entrance of light into the spectrographs. It is located remote from the spectrographs and is commanded separately from the VDAS computer. CCD integration period starting time (see Section 2.8) shall be able to be synchronized with the shutter operation to within 0.1 sec or better.

After receiving a Perform Exposure command (see requirements 10, 11, and 12 in Table 7) from the VDAS computer, the detector system shall automatically start the integration period at the requested time within 0.1 sec or better.

5.3 Instead of using the GPS-based network time appliance (which has a one pulse per second output signal) at the CCD controller level to facilitate synchronization of the detector system and shutter, the CCD controller's inherent response time to VDAS commands will be relied upon to achieve synchronization to within ±10 msec or better. To achieve the required level of synchronization, the CCD controller's response time to VDAS "Perform Dark Exposure" and "Perform Light Exposure" commands shall be constant to within ±10 msec or better.

5.4 CCD readout electronics shall automatically provide 32 overscan columns and 8 prescan pixels.

5.5 Integration period for an exposure shall be user selectable as follows:
- Zero seconds for a bias exposure
- Between 1.0 second and 3600 seconds in 0.1 second increments for all other types of exposures.

5.6 Integration period shall be able to be reset while an exposure is in progress.

5.7 Integration period shall be accurate to 0.1 seconds for non-bias exposures.

5.8 Full readout from shutter close to readiness for the next exposure shall be as per requirement 7.16.

5.9 CCD readout electronics shall be able to read all CCDs in parallel to minimize overhead.

5.10 CCD controller shall support user selectable binning as per requirement 3.17.

5.11 CCD controller read noise shall meet requirements 3.5 and 3.18.

5.12 Spurious charge is included in requirement 5.11, and shall be controlled to meet that requirement.

5.13 All of a CCD's on-chip amplifiers shall be serviced by the same controller. Additionally, each controller may service up to two CCDs.

5.14 If the CCDs are read out through two amplifiers the crosstalk between channels shall be $< 10^{-4}$ of the signal, with a goal of $< 10^{-5}$.

5.15 Crosstalk between channels contained in any two different CCDs shall be $< 10^{-5}$ of the signal.

5.16 The signal from each CCD shall be digitized to 16 bits with no missing codes. The median gain for the entire detector system shall be set somewhere between 1.0 and 1.2 electron per ADU digital number. The peak to peak variation (about this median) of all detectors in the system shall be within ±0.1 electron per ADU digital number.

5.17 Controller linearity shall meet requirement 3.9.

5.18 Space is available external to the cryostats for the controllers as shown in Figure 38 (note H ≤ 120 mm, D ≤ 250 mm, and W ≤ 200 mm. Additional space may also be available in other locations in the vicinity of the cryostats. Final location of the controllers and design of the cryostat shall be mutually agreed-upon.

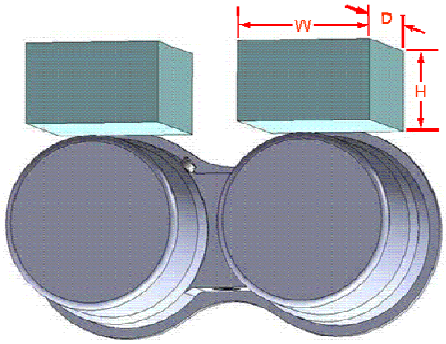

Figure 38: Controllers may be located outside the cryostats in the vicinity shown in this figure. Note that in this figure H ≤ 120 mm, D ≤ 250 mm, and W ≤ 200 mm.

5.19 The electrical interface between the CCD and CCD controller shall be mutually agreed upon as per HX0032. This includes defining the electrical parameters that must be adjustable via computer control.

6 Cryogenic and Vacuum Requirements

6.1 CCD temperature set point shall satisfy the requirements of Section 3 within the temperature control range. CCD operating temperature shall be selected by Contractor and shall be between -110°C and -90°C.

6.2 CCD temperature set point shall be set in firmware and shall be adjustable (via computer control in 0.1°C increments) over a ±10°C range that is centered on the nominal set point.

6.3 Detector system shall actively control CCD temperature (through heating) so as to maintain stability of the dark count, on-chip amplifier gain, and bias level to within 0.1°C (peak-to-peak) of the set point over 1 hour, 0.2°C (peak-to-peak) over a 24-hour period, 0.5°C (peak-to-peak) over a year. Note that this stability requirement does not include the long term drift of the temperature sensor.

6.4 Detector system shall use CBA heater and temperature sensors as part of a closed loop circuit to control CCD temperature. As an option, on-chip CCD temperature sensors may also be read and reported by the system.

6.5 Detector system shall be equipped with mutually agreed-upon electrical interfaces for the cold block heaters, cold block temperature sensors, and cold finger temperature sensors.

6.6 Detector system shall be able to measure cold block and cold finger temperatures with the accuracies as indicated in Table 6.

Temperature Range	Measurement Accuracy (°C)
-140°C to -120°C	±5.0°C
-120°C to -80°C	±1.0°C
-50°C to 40°C	±5.0°C

Table 6: Temperature measurement requirements.

6.7 Closed loop CCD temperature control shall be able to be turned "on" and "off" via computer control.

6.8 All detector system components (including adhesives and solder) that reside inside the cryostat shall be vacuum compatible with the vacuum levels stipulated in Table 10. Note that only flux-free solder is permitted inside the vacuum.

6.9 The average heat load on the cold block due to detector system components shall be minimized and limited to ≤ 0.4 Watt. This requirement is limited to the heat loads from the following:
- Vacuum electronics interconnect
- CCD (for a 300 second exposure time and 20 second readout time)
- All other detector system heat generating components inside the cryostat

6.10 Detector system shall be able to monitor all temperature sensors when the cryostat is being pumped down, cooled down, warmed up, and brought back up to ambient pressure.

7 Computer Hardware and Software Requirements

7.1 Detector system shall interface to a single VDAS computer via a mutually agreed-upon hardware/software interface. All control and communications between the detector system and VDAS computer shall be through this interface. Note that:
- Image data shall be received from the CCD controller by the VDAS computer which will format the data and then write it to disk
- The VDAS computer will collect appropriate data from the CCD controller and other sources and then create the FITS header

7.2 A detector system Application Programming Interface (API) shall be provided by the Contractor that allows the VDAS computer to control the detector system via mutually agreed-upon high-level calls, running under a mutually agreed-upon operating system (note that the preferred operating system is 64-bit Red Hat Enterprise Linux 5).

7.3 Software shall be provided that allows all detector system features to be tested. This test software shall run on the VDAS computer under a mutually agreed-upon operating system (see requirement 7.2), shall be equipped with a Graphical User Interface (GUI), and shall communicate with the detector system via the API specified above.

7.4 Detector system shall have a modular and scalable hardware and software architecture which facilitates addition of spectrographs in groups of 16.

7.5 Detector system hardware and software architecture shall be capable of supporting 192 CCDs. As a goal, the architecture shall support 256 CCDs.

7.6 Detector system shall be equipped with spectrograph enclosure slot address generators that have mutually agreed-upon electrical and mechanical interfaces.

7.7 Detector system hardware and software architecture shall support 96 unique slot addresses. As a goal, the architecture shall support 128 unique slot addresses.

7.8 Detector system shall be able to function with one or more spectrographs (including a single camera in a spectrograph pair) completely disconnected from the detector system and/or declared “Bad” by the VDAS computer system.

7.9 Detector system API shall, at a minimum, support the VDAS computer command set (or equivalent mutually-agreed upon command set) listed in Table 7.

7.10 Detector system API shall, at a minimum, have the ability to issue Table 7 commands to all CCDs/controllers and have them execute the command simultaneously.

7.11 Detector system API shall, at a minimum, have the ability to issue Table 7 commands to specific combinations of CCDs/controllers (which includes a single CCD), and have them (i.e., the specific CCDs/controllers) execute the command in parallel to minimize overhead.

7.12 Detector system shall support the user-settable parameters listed in Table 8. Table 8 parameters shall be set within one second after receiving a VDAS computer Set Parameter command. Note that the registers associated with these parameters shall also be readable.

7.13 Detector system shall support the measurements and inquiries listed in Table 9.

7.14 Get Parameter and Get Measurement commands shall specify which items to report for each hardware component (e.g., report all parameters and measurements for all hardware, or only report cold block temperature measurements for CCDs 10 through 15 and CCD 100).

7.15 Detector system shall report the requested information within one second after receiving Get Parameter and Get Measurement commands. In addition, these reports shall contain a "time stamp" that is accurate to within 0.1 seconds.

7.16 Detector system shall be capable of reading up to 192 CCDs, sending the data to the VDAS computer system, and then flushing the CCDs, all within ≤ 20 seconds when using 2 x 1 binning. At the end of this time period, the detector system shall be ready to start data acquisition upon receiving a Perform Exposure command (see Table 7 requirements 10, 11, and 12) from the VDAS computer system. Note that the readout time for 1 x 1 binning and 2 x 2 binning is not specified. Also note that, although not preferred, it is acceptable to provide a local frame buffer if necessary to meet the 20 second time requirement.

7.17 Each time a CCD is read out the following information shall be able to be reported as part of the CCD's read out data:
- CCD hardware ID (see item 1 in Table 9) and address
- Which amplifier was used to read the data (this is only required if each CCD has more than one on-chip amplifier (see requirement 3.19)
- Which spectrograph the CCD is installed in (i.e. the spectrograph enclosure slot address)
- Which firmware was used to read the CCD (see item 2 in Table 9)
- All unique identifiers for any other hardware components in the read out chain (see item 1 in Table 9)
- All unique identifiers for any other software components in the read out chain (see item 2 in Table 9)

7.18 Detector system shall be able to simultaneously flush some of the CCDs (i.e. the ones that have been exposed to bright objects in the previous observation) while all of the other CCDs are acquiring data (see requirement 3.14). Note that the VDAS computer system shall determine which CCDs need to be flushed during each data acquisition period.

Item	Command	Notes
1	Restart	Restart the detector system as per requirement 8.3 without power cycling the AC power to the detector system
2	Startup and Shutdown Specific Cameras	As required to support requirement 8.2
3	Turn Standby Mode On/Off	Safe standby mode to be specified by Contractor
4	Specify Detector Subset	Specifies which subset of detectors are acted upon by VDAS computer commands listed in Table 7
5	Set Parameter	See requirement 7.12 and Table 8
6	Get Parameter	See requirement 7.12 and Table 8
7	Get Measurement	See requirement 7.13 and Table 9
8	Flush Once	See requirement 5.1
9	Flush Continuously	See requirement 5.1
10	Perform Light Exposure (Start Time)	This command is executed as described in Section 2.8. Also note that the Start Time input parameter is optional. If the Start Time is not specified the integration period shall start within 0.1 seconds after the command is issued.
11	Perform Dark Exposure (Start Time)	A dark exposure is the same as a light exposure but the shutter remains closed
12	Perform Bias Exposure (Start Time)	A bias exposure is a dark exposure with a zero second exposure time
13	Abort Exposure	Stop the exposure without reading the CCDs and flush the CCDs
14	Pause Exposure	Pause the detector system integration timer until a Resume Exposure command is received. Note that the VDAS computer will also close the shutter when a Pause Exposure command is issued.
15	Resume Exposure	Resumes a paused exposure by restarting the integration period timer. Note that the VDAS computer will also open the shutter when a Resume Exposure command is issued.
16	Other Commands	Other commands as needed that are not mentioned above (e.g., to set hardware parameters, etc)

Table 7: Detector system commands.

Item	Parameter	Notes
1	CCD Binning Parameters	See requirements 3.17 and 5.10
2	Integration Period	See requirements 5.5 and 5.6
3	CCD Temperature Set Point	See requirement 6.2
4	CCD Temperature Control On/Off	See requirement 6.7
5	Spectrograph Status	See requirement 7.8
6	Any Other User-Settable Parameters	

Table 8: User-settable detector system parameters which can also be read by the VDAS computer system.

Item	Measurement	Notes
1	Hardware ID	Unique identifier with revision number for all hardware components including CCDs, controllers, and auxiliary controllers
2	Software ID	Unique identifier with revision number for all software and firmware residing in the detector system and VDAS computer
3	Spectrograph Enclosure Slot Address	
4	Cold Finger Temperature Sensor Measurement	
5	Cold Block Temperature Sensor Measurement	
6	Cold Block Heater Current	Precision shall be sufficient to detect a heater power change of ≤ 10 mW
7	Cold Block Temperature Servo Error Signal	Difference between the cold block actual temperature and requested temperature
8	Any Other Available Diagnostic Information	For example, critical CCD voltages and currents

Table 9: Measurements and inquiries that can be made with the detector system.

8 Electrical Requirements

8.1 Detector system shall operate off of a mutually agreed-upon University supplied DC power supply with mutually agreed-upon specifications.

8.2 It shall be possible to turn off and remove a spectrograph pair (with associated detector system components) as a complete assembly without affecting the operation of the other detector system components.

8.3 After power has been applied as per requirement 8.1, the detector system shall automatically start up without human intervention. This includes establishing communication with the VDAS computer and other detector system components. At the end of the start-up period the detector system shall be in Standby Mode (see item 3 in Table 7).

8.4 Detector system shall automatically failsafe without damage to the CCDs and other detector system electronics when the following events occur:
1) Loss of DC power for any duration
2) DC power over-voltage, under-voltage, over-current
3) Power supply failures
4) Improper CCD clock voltages (as a goal)
5) CCD clock sequences that could result in damage to the CCDs (as a goal)
6) Disconnecting interconnection cables while system is powered (as a goal)
7) Indirect lightning strike (as a goal).
Note that to meet requirements 3 through 7, the system may contain sacrificial components that are inexpensive and easy to replace.

8.5 Detector system shall automatically shutdown without damage to the CCDs and other detector system electronics when the following events occur:
1) Loss of DC power for any duration
2) DC power over-voltage, under-voltage, over-current
3) Any combination of the above when applied cyclically for extended durations.
Note that DC power to the detector system may be intentionally turned off to prevent damage from external events which are automatically detected by other Observatory safety systems.

8.6 Detector system (hardware and software) shall recover from an improper shutdown (e.g. unexpected loss of electrical power) within a reasonable time frame (say less than 10 minutes) with at most the assistance of a single individual that has a high school education and has been trained to follow your recovery procedure. A goal is to make it so that the operator does not have to manually delete temporary files and reset counters, etc. to facilitate the recovery.

8.7 All detector system interconnects between the spectrograph enclosures and upper electrical room shall be via fiber optic cables that are routed through the telescope cable wrap. Cable connector diameter shall not exceed 50 mm. Cross sectional area of all detector interconnects in the cable wrap shall not exceed 13 cm^2.

8.8 If contractor's bid includes the fiber optic cables between the spectrograph enclosures and upper electrical room, a spare fiber optic cable shall be provided for each of the fiber optic cables associated with requirement 8.7.

8.9 If contractor's bid includes the fiber optic cables between the spectrograph enclosures and upper electrical room, three patch panels for the fiber optic cables associated with requirement 8.7 shall be provided at the following locations:
- One patch panel in the upper electrical room at a mutually-agreeable location in the vicinity of the VDAS computer
- One patch panel in each of the spectrograph enclosures at a mutually-agreeable location

8.10 All fiber optic connectors between field replaceable detector system components shall be LC and ST style connectors, and shall:
- be environmentally sealed (IP65 or better)
- have a protective cap with swivel lanyard
- be equipped with strain relief

8.11 All electrical connectors between field replaceable detector system components shall be circular Military Spec connectors (or mutually agreed-upon functional equivalent) with the following features:
- Environmentally sealed (IP65 or better)
- Protective cap with swivel lanyard
- Keyed

- Bayonet type
- Equipped with strain relief
- Pin count ≤ 50.

8.12 Detector system components shall not degrade performance or functionality of any of the other detector system components regardless of their location (e.g., upper electrical room, spectrograph enclosure 1, and spectrograph enclosure 2).

8.13 Standard and recommended practices (see for example References 10, 11 and 12) for distribution of AC and DC power and ground, separation of power and signal cabling in the enclosures, and shielding of signal carrying cables shall be followed as applicable.

8.14 Detector system components (including the power supplies supplied by the University) that are located in the bottom of each spectrograph enclosure shall fit within the equivalent of eight 19" wide by 10U (i.e., 17.5") high by 23.88" (i.e., 606 mm) deep equipment racks that are located side by side.

9 Vacuum Electronics Interconnect Requirements

9.1 Vacuum electronics interconnect shall be a flex circuit (or equivalent) that is equipped with appropriate stiffeners and attachment points.

9.2 The portion of the interconnect that spans the gap between the CCD and cryostat housing shall be self-supporting and shall be painted with ALION MH2200 to control stray light. Note that it is acceptable to provide a cover that is painted with ALION MH2200 (or equivalent) to eliminate the need to paint the interconnect, provided the cover is within the geometric envelope described in requirement 11.3.

9.3 The interconnect circuit shall be shielded (with ground layers as appropriate) to provide electrical shielding of sensitive signals.

9.4 One side of the interconnect shall be soldered to the cryostat bulkhead connector. The other side shall be soldered (or bond wired) to the CCD and, as a goal, the other side shall also be soldered to the cold block heater, cold block temperature sensor, cold finger temperature sensor, and other detector system components that are located inside the cryostat. Otherwise a reliable connector shall be used.

9.5 Vacuum electronics interconnect dimensions and circuit length shall be made as small as reasonably practical, subject to the vacuum cryostat's geometric constraints.

10 Bulkhead Connector Requirements

10.1 Each vacuum cryostat services two spectrographs. Each spectrograph has its own CCD, cryostat temperature sensor, cold block temperature sensor, and cold block heater. As a goal, electrical interconnect to each spectrograph's CCD, cryostat temperature sensor, cold block temperature sensor and heater, shall be via a single male bulkhead connector. If a single connector is not possible, a maximum of three connectors may be used per spectrograph.

10.2 Bulkhead connectors shall be as per requirement 8.11.

10.3 Bulkhead connector shall be attached to the cryostat so as to allow the spider assembly to be removed from the cryostat without disconnecting the bulkhead connector from the vacuum electronics interconnect.

10.4 Mechanical interface between the bulkhead connector and cryostat shall form a vacuum seal.

10.5 Bulkhead connector shall be able to be removed from the cryostat housing without disconnecting the electrical interconnect from the detector head subassembly.

10.6 All electrical connections to the vacuum side of the bulkhead connector shall be soldered.

10.7 When a bulkhead connector is not connected to its mating connector, the connector's exposed pins may be subject to ESD from external sources. ESD created by touching exposed bulkhead connector pins shall not damage the CCD associated with that connector.

10.8 When a bulkhead connector protective cap is deployed (i.e., installed) it shall electrically connect all of the bulkhead connector pins to one another (i.e., short all of the pins to one another), to prevent damage to sensitive electronics caused by the electrostatic discharge.

10.9 Bulkhead connector dimensions shall be made as small as reasonably practical within project cost and physical constraints.

11 Optical Obstruction and Stray Light Requirements

11.1 Bulkhead connectors shall not prevent light within the optical clear aperture entering the camera from reaching the camera's spherical mirror.

11.2 Vacuum electronics interconnect shall lie within the optical obstruction caused by the spider arm and back cap (see Figure 30).

11.3 The CCD shall ideally fit within the geometric envelope shown in the left side of Figure 39, where L1 = 47 mm, H1 = 58 mm, and A = 10°. Note that H1 cannot be larger than 100 mm, and is limited by the position of the corrector plate window.

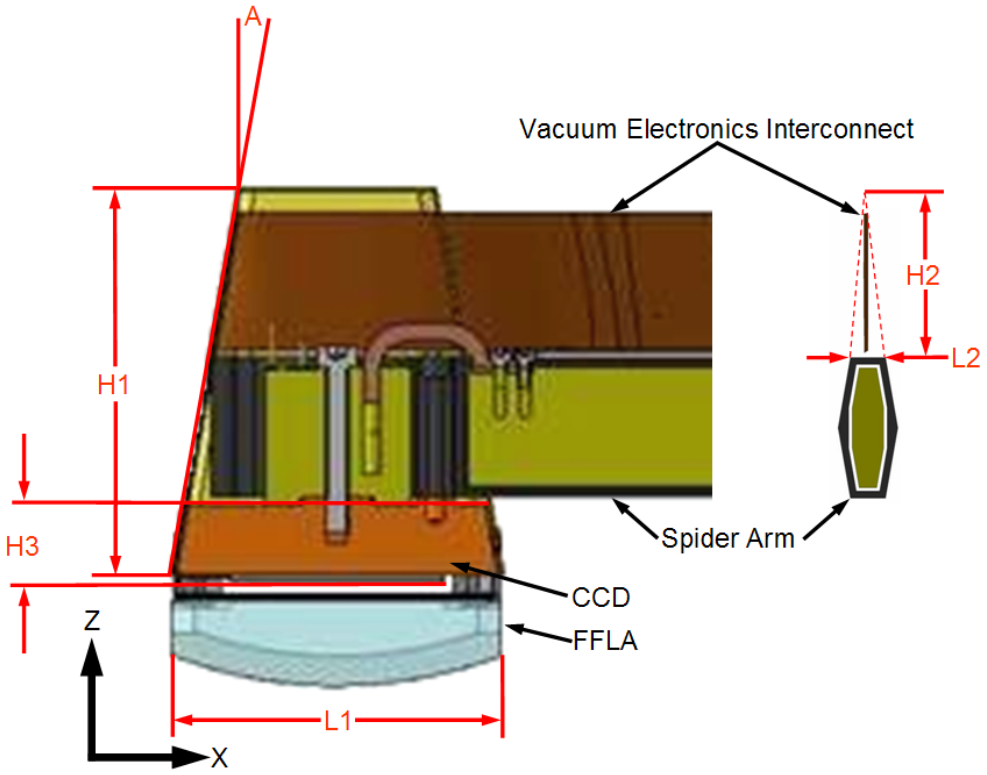

Figure 39: Detector system geometric envelope. The left side of this figure is a cutaway view through the XZ plane. The values of A, H1, and L1 in the YZ plane are identical to those in the XZ plane.

11.4 As a goal the vacuum electronics interconnect shall fit within the triangular envelope shown in the right side of Figure 39, where L2 is equal to 5 mm, and H2 is ideally 14 mm but could be as large as 20 mm. Any detector system components outside this envelope shall be mutually agreed upon.

11.5 The distance between the CCD active surface and interface to the CBA (i.e. dimension H3 in Figure 39) shall be 11 mm.

11.6 The vacuum electronics interconnect and other electronics to support the CCD (e.g., the ASIC mentioned in Section 2.3) shall fit within the annular region shown in Figure 40 where R1 = 133 mm and R2 = 100 mm.

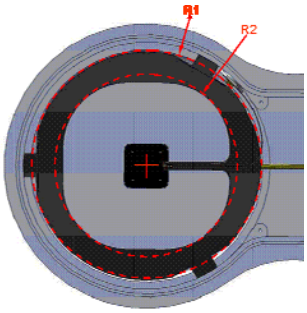

Figure 40: Detector system geometric envelope.

11.7 Use of phosphorescent, fluorescent, and radioactive materials shall be avoided for all detector system components located inside the cryostat. Detected alpha, beta, and gamma emissions from materials shall total less than the expected dark current.

11.8 All detector system components located inside the cryostat shall not emit light within the CCD sensitivity bandwidth (i.e., between 200 nm and 1.2 μm).

11.9 The portion of the vacuum electronics interconnect that passes through the optical beam path (Figure 27) shall be painted with ALION MH2200 (or mutually agreed-upon equivalent) to control stray light.

11.10 All detector system components which are exposed directly to the primary optical beam or indirectly to stray light, shall be painted with ALION MH2200 (or mutually agreed-upon equivalent) to control stray light. If this is not possible, these components shall be baffled by components that have been painted with ALION MH2200 (or mutually agreed-upon equivalent).

11.11 All detector system components located inside the telescope dome (which includes components located inside the spectrograph enclosures) shall not emit light (within the bandwidth between 350 nm and 1.8 μm) into the dome and spectrograph enclosures.

12 Environmental Requirements

12.1 Detector system shall meet all specifications for any combination of the Normal Conditions shown in Table 10. Detector system shall survive any combination of the Normal Conditions without damage or requirement for repair, realignment, and recalibration.

12.2 Detector system shall be able to operate (at reduced performance as specified by Contractor) for any combination of the Service Conditions shown in Table 10. Detector system shall survive any combination of the Service Conditions without damage or requirement for repair, realignment, and recalibration.

12.3 Detector system shall withstand any combination of the Survival Conditions shown in Table 10 when they are not operating. Detector system shall survive any combination of the Survival Conditions without damage or requirement for repair, realignment, and recalibration.

12.4 Detector system shall survive any combination of the Shipping Conditions shown in Table 10 without damage or requirement for repair, realignment, and recalibration, when packaged in their shipping containers and being transported by truck (non air ride), train, ship, and plane.

12.5 There are a variety of broadband and narrow band radiofrequency sources within the dome and upper electrical room. Table 11 lists some of these radio frequency sources. The detector system shall be able to operate and meet all performance specifications in the presence of these radio frequency sources. Note that this only applies when the detector system components are installed at the facility (e.g., when the cameras are installed inside the spectrograph enclosures). Contractor shall use best practices to minimize detector system sensitivity to conducted and radiated interference.

12.6 All parts of the detector system (that are external to the cryostats) that require liquid cooling (e.g. glycol and water) shall be able to safely withstand cooling leaks without damage or requirement for repair.

Quantity	Normal	Service	Survival	Shipping
Elevation	Sea level to 2026 m	Sea level to 2026 m	Sea level to 2026 m	Sea level to 11000 m
Cryostat vacuum	10^{-5} mbar to 10^{-7} mbar	1 ATM to 10^{-7} mbar	1 ATM to 10^{-7} mbar	NA
Maximum rate of cryostat vacuum pressure change	1 ATM/yr	0.04 ATM/min	0.1 ATM/min	NA
Temperature	As per requirement 6.1 IC -10°C to 30°C IE, ID & IU	-5°C to 35°C IC -10°C to 35°C IE, ID & IU	-140°C to 45°C IC -25°C to 45°C IE, ID & IU	-25°C to 66°C
Maximum rate of temperature change	2°C per min IC 1°C per hour IE, ID & IU	2°C per min IC 1°C per hour IE, ID & IU	10°C per hour	42°C per hour
Relative humidity	0.0% IC ≤ 95.5% non condensing IE, ID & IU	0.0% IC ≤ 95.5% non condensing IE, ID & IU	≤ 100% condensing OC	≤ 100% condensing
Accelerations generated when HET is rotating about its azimuth axis	0.1 g tangential 0.5 g radial	Best practices	Best practices	NA
Gravity orientation	Constant	Any orientation	Any orientation	Any orientation
Vibration	NA	Best practices	Best practices	MIL-STD-810F, Jan 2001
Shock	NA	Best practices	Best practices	Drop Height (mm) 914 (package 0 to 13 kg) 762 (package 13 to 34 kg) 457 (package 35 to 64 kg)
Seismic (peak acceleration)	NA	NA	0.2 g in any direction	NA
Wind blown dust, sand & insects	NA	NA	Yes ID	Yes

Table 10: Detector system environmental conditions (IC = Inside Cryostat, OC = Outside Cryostat, IE = Inside Spectrograph Enclosure, ID = Inside Dome, IU = Inside Upper Electrical Room).

Item	Description	Location	Approximate Frequency
1	Handheld Radios	ID & IU	151 MHz
2	Cellular Telephones	ID & IU	
3	Dome Crane Wireless Control		400 MHz
4	SAMS	ID	5th harmonic @ approximately 400 MHz
5	Dome Shutter Wireless Control		900 MHz
6	Wireless Ethernet		1.5 GHz
7	Electric Motors	ID	Broadband
8	Switching Power Supplies	ID & IU	Broadband
9	High-speed Clock Signals	ID & IU	Broadband

Table 11: Example radio frequency sources inside the dome and upper electrical room (ID = Inside Dome, IU = Inside Upper Electrical Room). The use of radios, cellular telephones, dome crane wireless control, and dome shutter wireless control is intermittent and typically does not occur when the detector system is being used to acquire astronomical data.

13 Reliability, Maintainability, and Servicing Requirements

13.1 The detector system shall have a design lifetime of 20 years. This assumes that the system is maintained as per the manufacturer's recommendations as provided in the Maintenance Manual, and that the recommended spares have been purchased to support the manufacturer's recommended spares strategy.

13.2 Detector system shall be capable of operating 365 nights per year.

13.3 Detector system Mean Time Between Failure (MTBF) shall be at least 672 hours (i.e., 28 days of continuous operation). Note that this MTBF is for the entire detector system with 192 cameras.

13.4 Detector system Mean Time to Repair (MTTR) shall be no more than ten hours. As a goal MTTR shall be ≤ 4 hours. Note that this MTTR assumes:
- Failures are only isolated down to the field-replaceable module level
- Components inside the vacuum cryostats do not have to be replaced
- An adequate supply of field-replaceable spares is on site.

13.5 Components with low MTBF (e.g., muffin fans) shall be readily accessible and easy to replace.

13.6 All components shall be protected from corrosion by proper surface treatment (e.g., anodizing and painting).

13.7 Metric fasteners shall be utilized whenever possible.

13.8 Commercial off the shelf equipment with short lead time shall be used whenever possible to reduce the onsite spares inventory.

13.9 System shall be designed to minimize the need to tune/calibrate components in situ. As a goal, all adjustments required to tune/calibrate detector system components will be via computer control.

13.10 Whenever possible, all electronic writeable registers shall be readable to facilitate troubleshooting.

13.11 Spares shall have a ten-year shelf life when stored as per the manufacturer's recommendations.

13.12 Detector system equipment (excluding interconnects, items inside the cryostats, and items mounted to the outside of the cryostats) located inside the spectrograph enclosures shall be equipped with slides for rack mounting.

13.13 Detector system equipment (excluding interconnects and interface cards located inside the VDAS computer) located inside the upper electrical room shall be equipped with slides for rack mounting.

13.14 Detector system components (including CCDs and excluding interconnects) shall be marked with unique serial numbers. Serial number format, location, and orientation shall be mutually agreed upon. Additionally:

- Each CCD shall have a unique mark on the package and flex circuits shall be electronically encoded.
- CCD serial numbers shall be visible/readable after the back cap has been removed from the spider assembly.
- The flex circuit does not have to have a serial number label on it.

13.15 As a goal, all interconnect cable connectors and mating receptacles at each chassis shall be keyed differently to ensure that these cables cannot be connected to the wrong chassis receptacle.

13.16 All interconnect cable ends and mating receptacles shall be equipped with unique labels. These labels shall correspond to the identifiers used in the Maintenance Manual interconnect diagram. Label wording, location, and orientation shall be mutually agreed upon.

13.17 All markings and labels shall:

- Be protected from "rubbing off"
- Not fade (i.e., they must be legible over the system's design lifetime (see requirement 13.1)
- Not be able to be "peeled off"
- Be vacuum compatible where appropriate.

13.18 As a goal, readily accessible test points shall be provided at mutually agreed-upon locations. This includes test points for checking all power supply input and output voltages.

13.19 Tie mounts shall not be secured with adhesive.